EK-0TM03-TM-002

TM03 Magnetic Tape Formatter Technical Manual

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CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The TM03 Magnetic Tape Formatter serves as an interface between various magnetic tape transports and any Massbus controller. It provides control, data, status, and error information between the Massbus controller and a standard 1.27 cm (1/2 inch) magnetic tape unit (slave) operating at 114.3, 190.5, or 317.5 cm/second (45, 75, or 125 in/second). The TM03 is capable of reading and writing magnetic tape for information interchange at 800 bits/inch NRZI or 1600 bits/inch PE (phase encoded). It also has a forward and reverse read and spacing capability. The TM03 formats data from the PDP-10 and PDP-11 processors* into tape frame characters and performs the reverse during a data read operation.

Aside from providing magnetic tape formatting, the TM03 offers the following features.

1. The TM03 provides automatic error correction of single-track errors in PE data (hardware controlled).
2. The TM03 provides automatic error correction of single-track errors in NRZI read data. (NRZI error correction is under software control and therefore does not occur automatically as does PE error correction.)
3. The TM03 provides automatic selection of either 800 bits/inch (NRZI) or 1600 bits/inch (PE) density during a read operation from BOT (beginning of tape).
4. The TM03 is capable of controlling from one to eight slaves. It should be noted that although the TM03 can handle tape speeds of 114.3, 190.5, and 317.5 cm/second (45, 75, 125 in/second), all slaves interfaced to any one TM03 must be operating at the same tape speed.
5. The TM03 writes an industry-compatible PE tape mark.
6. The TM03 performs extensive parity checking throughout all read and write data paths. In addition, the TM03 is equipped with self-contained maintenance mode operations which allow complete testing of all critical electronics under diagnostic control.

1.2 GENERAL DESCRIPTION

Figure 1-1 illustrates a TM03/tape transport system configuration. Each TM03 can control up to eight slave transports. In turn, each Massbus controller can control up to eight TM03 formatters. Thus, a maximum of 64 tape transports could be interfaced to a single Massbus controller.

Figures 1-2, 1-3, and 1-4 show the TM03 in typical transport environments. An H740-DA power supply is required to provide power for the TM03. Figure 1-5 illustrates the TM03 front panel. A POWER indicator illuminates when power is applied to the TM03 from the H740-DA power supply. The PHASE ENCODED indicator illuminates when the TM03 is in the PE mode during a read or write operation.

*Also the PDP-15 via a PDP-11 for interface to the Massbus (PDP-15 Unichannel).

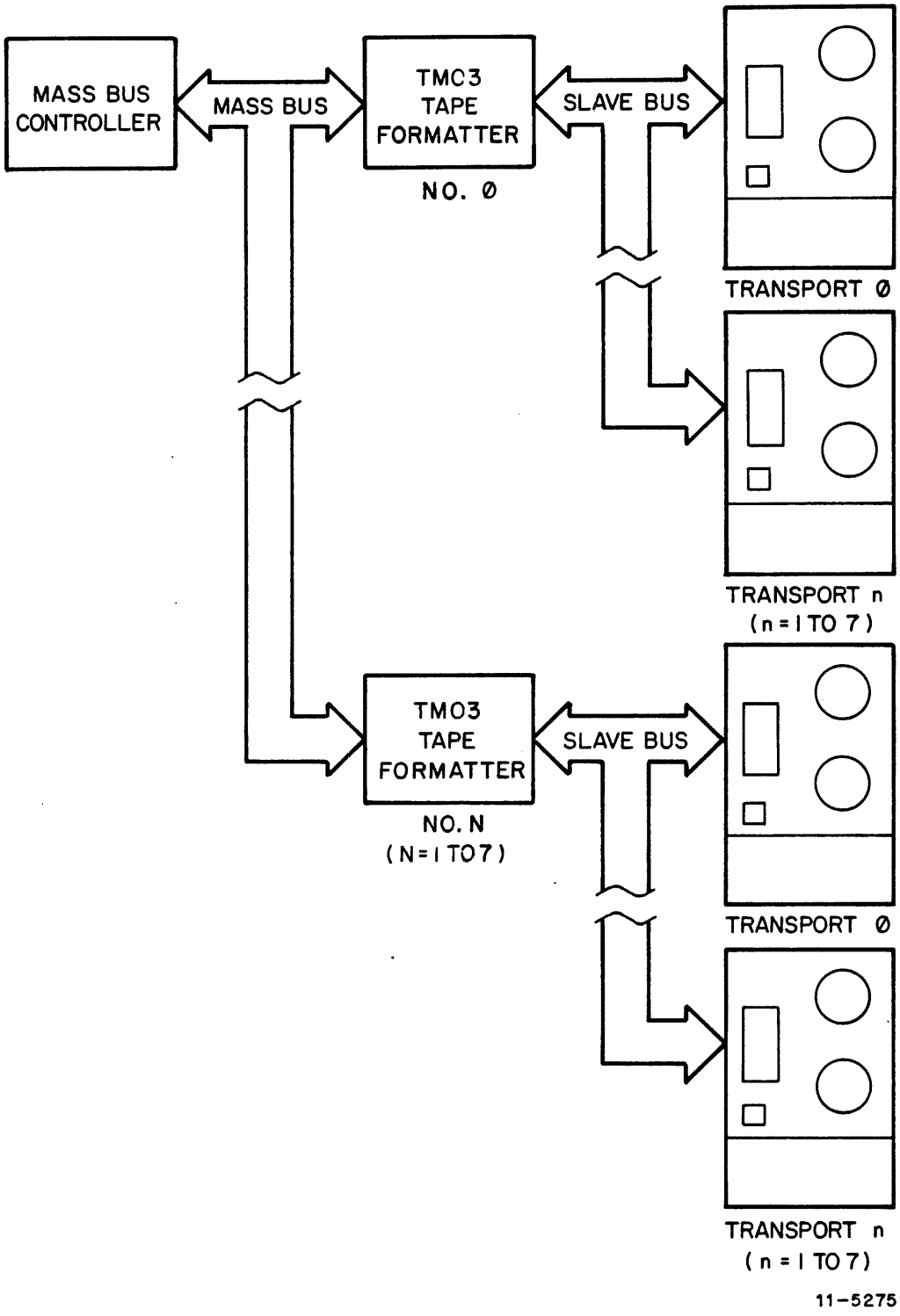


Figure 1-1 TM03 Tape Transport System Configuration

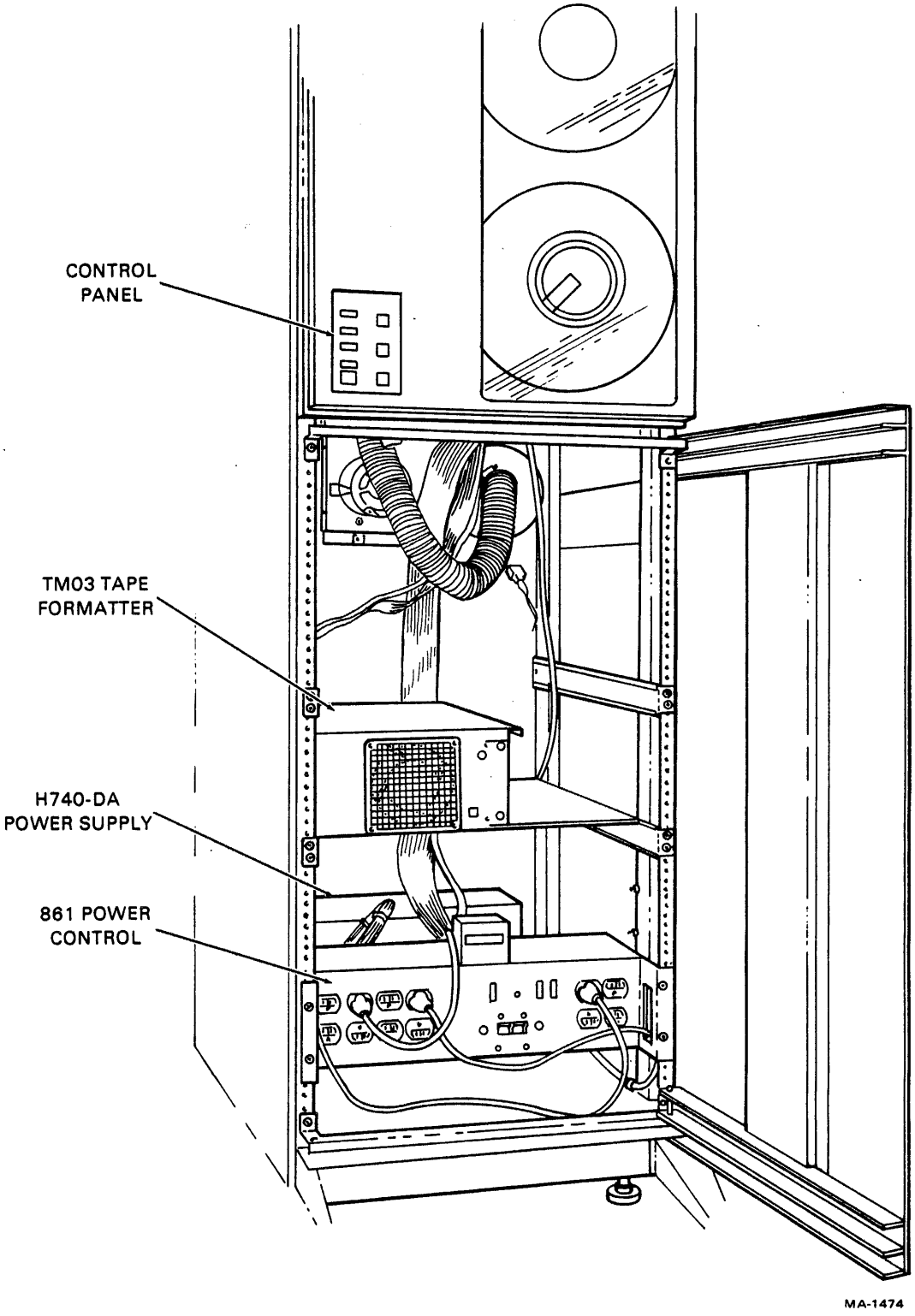


Figure 1-2 TM03 with TE16 Tape Transport in H950 Cabinet

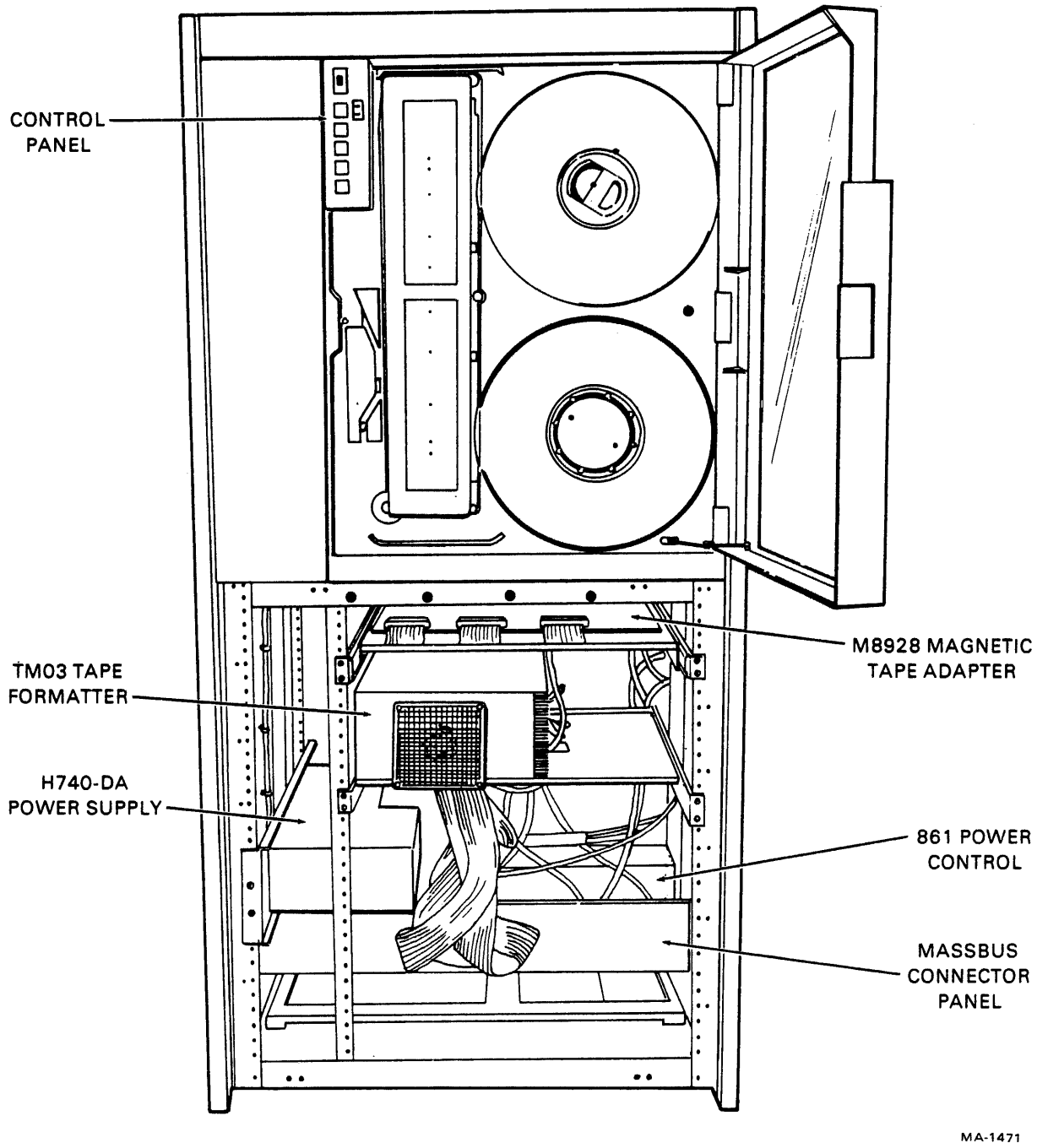


Figure 1-3 TM03 with TU45 Tape Transport in H9500 Corporate Cabinet

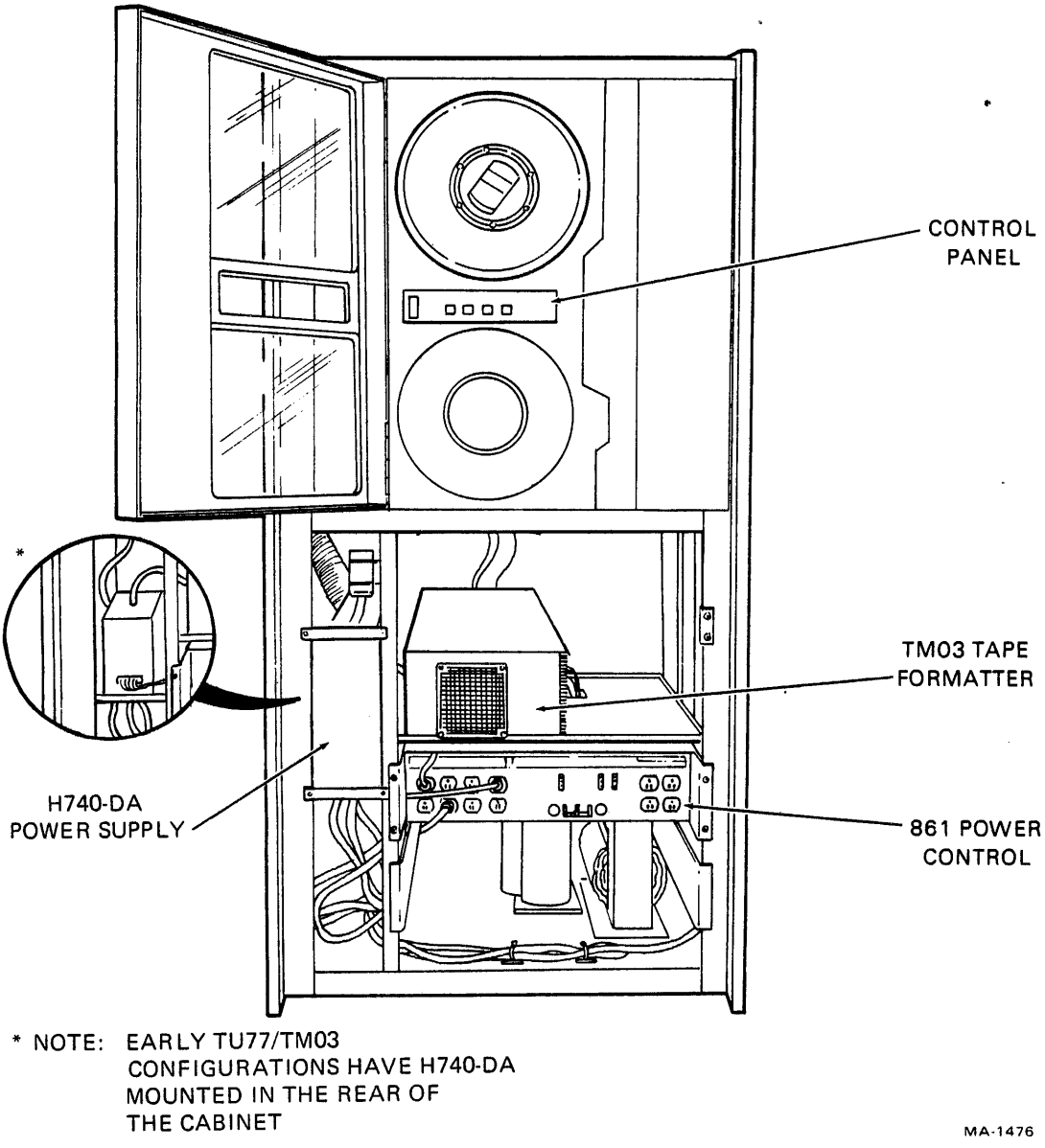


Figure 1-4 TM03 with TU77 Tape Transport in H9500 Corporate Cabinet

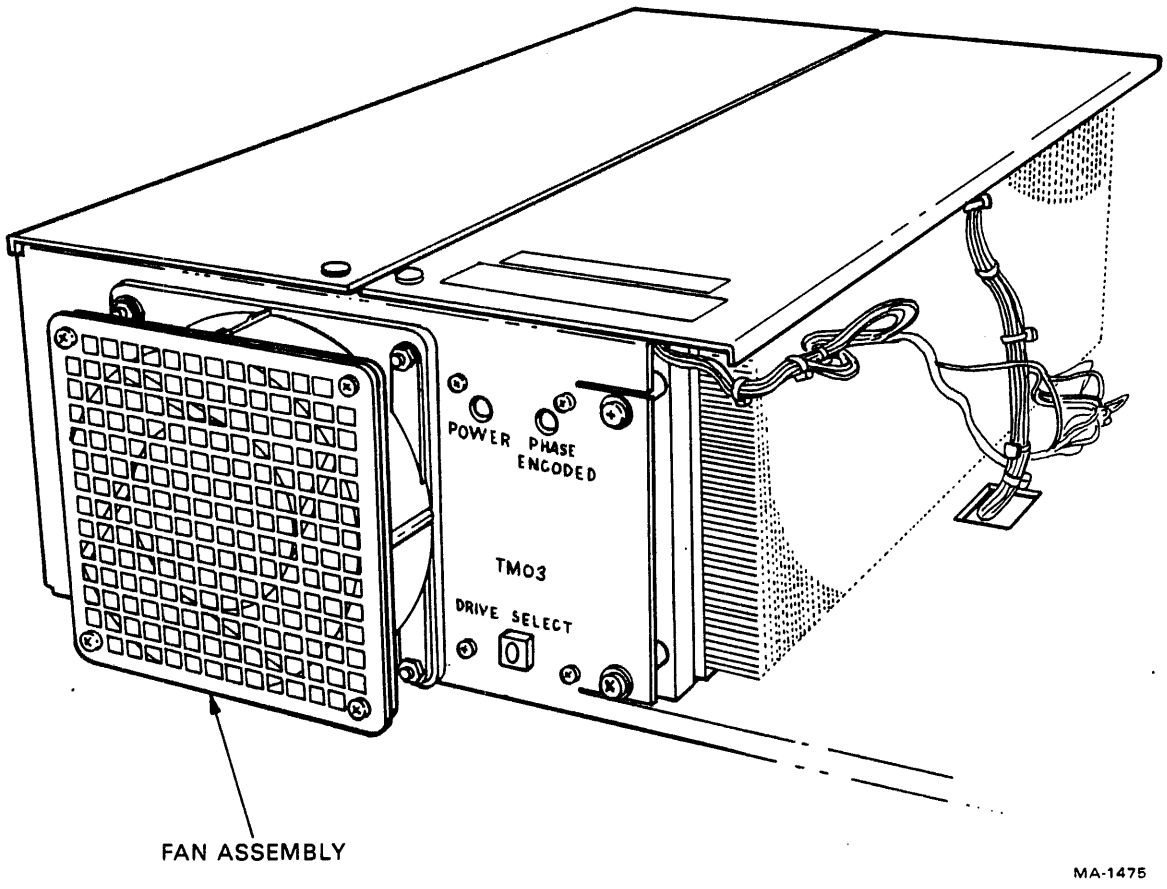


Figure 1-5 TM03 Front Panel

1.3 FUNCTIONAL DESCRIPTION

1.3.1 Introduction

The TM03/tape transport system (Figure 1-6) interfaces with the central processor unit (CPU) via the Massbus controller. However, the Massbus controller is almost transparent to the CPU, and the CPU operates as though it were controlling the drive directly.

The TM03 interfaces with the Massbus controller via the Massbus. The Massbus consists of an asynchronous control bus with its associated control lines, and a synchronous data bus with its associated control lines. Transactions on the control bus control the TM03/transport and determine its status, while transactions on the data bus transfer data to or from the TM03/transport. Because the data and control buses operate independently, the Massbus controller can monitor drive status while a data transfer operation is being performed.

The TM03 can control up to eight tape transports via the slave bus. All transports controlled by a TM03 are "daisy-chained" on the slave bus (Figure 1-6). Essentially, this means that the transports are configured in parallel to each other. The slave bus consists of slave select lines, write data lines, read data lines, transport control lines, and various transport status lines.

1.3.2 System Operation

Figure 1-7 is a block diagram of the TM03, and shows the major functional groups, control lines, and data paths. The following paragraphs describe these functional groups.

1.3.2.1 Massbus Interface Module (M8909-YA) – The Massbus interface module interfaces the TM03 with the Massbus controller. It contains circuitry that decodes the drive select signals on the Massbus. If enabled by the proper drive select address code, the Massbus interface can carry on the "handshake" operations with the Massbus controller, which read and write TM03 registers. The most important of the TM03 registers is the control register (CS1), which is located in the Massbus interface. The Massbus controller writes the function code of the next operation to be performed into the control register. The Massbus interface decodes this register and generates the appropriate control signals (FWD, REV, RWND, WRITE) to control the slave and various TM03 functions.

The Massbus interface module contains several other registers including an error register and a frame count register. The frame count register must be loaded prior to a space or write operation with the number (in 2's complement form) of records to be spaced or tape characters to be written. This register is incremented as the operation proceeds, and will terminate the operation with register overflow.

The Massbus interface decodes the control register to determine that a data transfer operation is to be performed. When this is the case, it generates OCC on the Massbus to notify the controller and other drives that it has occupied the data bus, and enables the bit fiddler.

1.3.2.2 Bit Fiddler Module*– The bit fiddler interfaces the TM03 data paths to the Massbus controller; it contains circuitry that performs synchronous data transfers on the data bus of the Massbus.

The bit fiddler is enabled for operation by the Massbus interface with BF ENABLE. The mode of bit fiddler operation is determined by control lines FMT0–3 (tape character format), WRITE (direction of transfer, i.e., read or write), and FWD (direction of tape motion, i.e., forward or reverse). WRITE and FWD are decodes of the control register function bits. FMT0–3 are the tape control register format bits, and are decoded in the bit fiddler.

*M8915-YA, M8915, or M8906, depending on processor and transport.

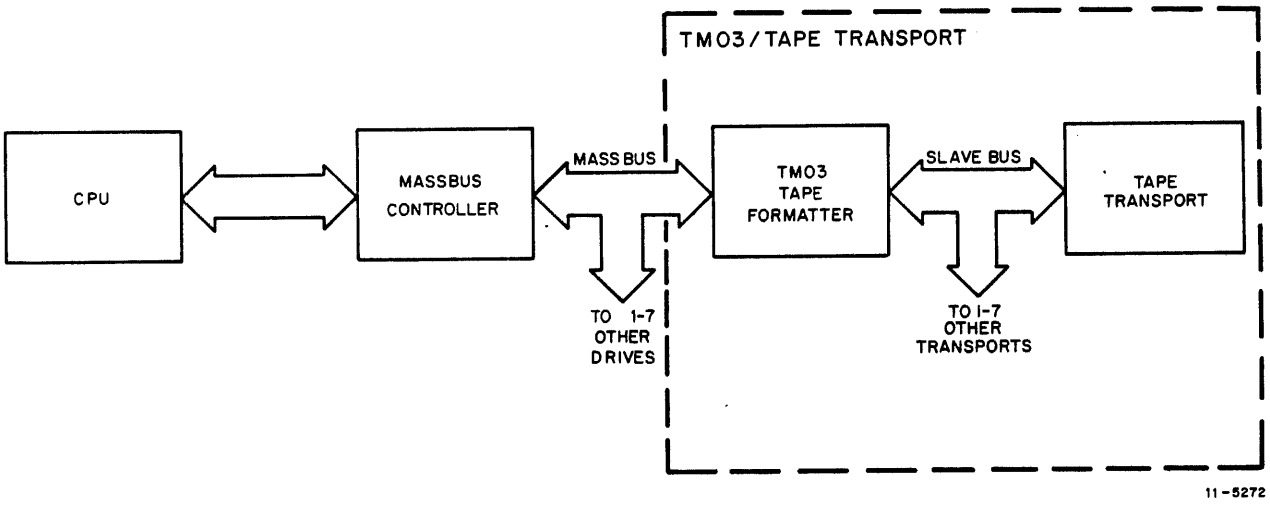
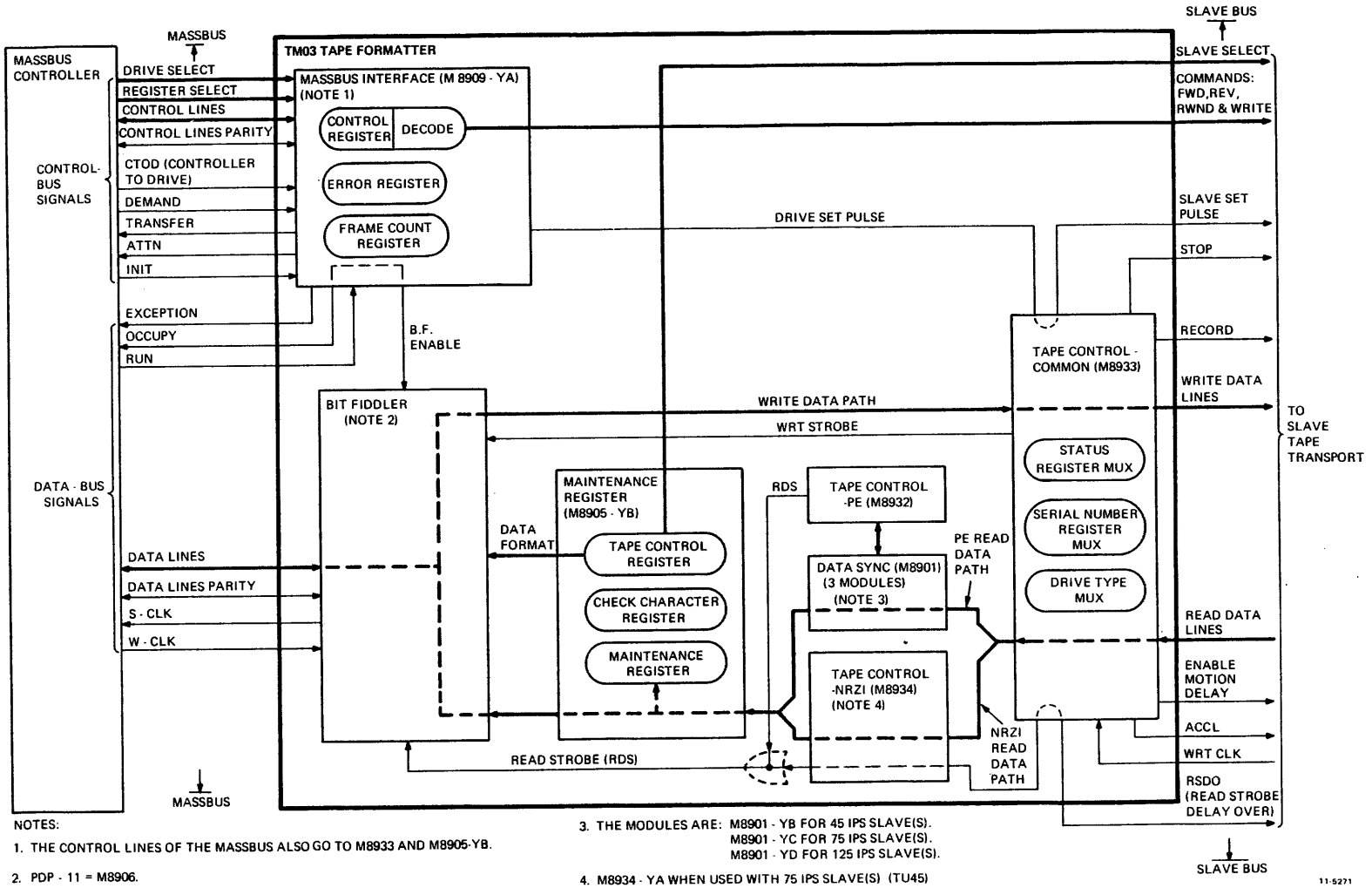


Figure 1-6 TM03 in a System Configuration



NOTES:

1. THE CONTROL LINES OF THE MASSBUS ALSO GO TO M8933 AND M8905-YB.
2. PDP - 11 = M8906.
   PDP - 10 = M8915 - YA (MAY BE M8915 EXCEPT FOR 125 IPS TRANSPORT (TU77) WHICH MUST USE M8915 - YA).
3. THE MODULES ARE: M8901 - YB FOR 45 IPS SLAVE(S).
   M8901 - YC FOR 75 IPS SLAVE(S).
   M8901 - YD FOR 125 IPS SLAVE(S).
4. M8934 - YA WHEN USED WITH 75 IPS SLAVE(S) (TU45)

Figure 1-7 TM03 Basic Block Diagram

During a write operation, the Massbus controller places a data word on the data bus. When the bit fiddler is ready to accept this data word, it issues SCLK (sync clock) to the controller, which replies with WCLK (write clock).

Upon receiving WCLK, the bit fiddler strobes in the word on the data bus, performs a data bus parity check, disassembles the data word into 8-bit characters, and generates a vertical parity bit for each 8-bit character. After generating WCLK, the controller places the next data word on the data bus. When the bit fiddler has finished disassembling the previous data word, it issues another SCLK, receives another WCLK, and strobes in the next data word for disassembly. The process continues until all the data has been transferred (precluding occurrence of data errors or other failures).

During a read operation, the bit fiddler assembles 8-bit characters into data words. When the data word has been assembled, it is placed on the data bus along with a parity bit (DPA), and the bit fiddler generates an SCLK pulse. When the Massbus controller receives SCLK, it strobes in the data on the data bus. The bit fiddler continues to assemble data characters into data words, and notifies the controller that a data word is available by generating SCLK. As in a write operation the method of assembly is determined by the FMT0–3, WRITE, and FWD signals input to the bit fiddler.

1.3.2.3 Maintenance Register Module (M8905-YB) – The maintenance register module is part of the read data path; read data is multiplexed through the maintenance register module from the PE or NRZI read circuitry (M8901 or M8934) to the bit fiddler. The maintenance register module also contains the tape control register, the check character register, and the maintenance register. The tape control register contains slave select bits, which are translated to slave bus signals (SS 0–2) and determine which slave will perform the operations specified by the Massbus controller. This register also contains tape data format information. Therefore, the tape control register must be properly loaded by the Massbus controller prior to the specification of a particular functional operation.

The maintenance register module plays an important role in maintenance mode operation. By writing into the maintenance register (R03), the Massbus controller can select one of several maintenance modes. These modes allow:

1. Testing of various TM03 circuits independently of the slave transport
2. Testing of the TM03 under tighter operation criteria.

1.3.2.4 Tape Control-NRZI Module (M8934)* – The tape control-NRZI module performs functions relating only to NRZI data storage and retrieval. During an NRZI read operation, the tape control-NRZI module is part of the read data path. When informed by the slave that a tape character is available [RSDO (read strobe delay over) asserted], the tape control-NRZI module generates RDS (read strobe) and strobes the tape character from the tape control common mode module (M8933) into an NRZI read latch. The output of the latch, multiplexed through the maintenance register module, becomes available to the bit fiddler.

During an NRZI read operation, the tape control-NRZI module also generates and checks LRCC (longitudinal redundancy check character) and CRCC (cyclic redundancy check character), checks vertical parity, detects tape marks (file marks), performs error correction of single track errors if the software so specifies, and determines that the minimum criteria for normal termination have been met.

During an NRZI write operation, the tape control-NRZI module generates the CRCC.

*M8934 for 114.3 cm/second (45 inch/second) and 317.5 cm/second (125 inch/second) slaves (TE16 and TU77). M8934-YA for 190.5 cm/second (75 inch/second) slaves (TU45).

1.3.2.5 Data Sync-PE Module (M8901)* – The data sync module (one of three) is part of the PE read data path. It processes PE read data from the tape control common mode (TCCM) module (M8933), converting the PE information to binary and deskewing the data. It operates with the tape control-PE module (M8932) to detect preamble, data, postamble, and tape mark (TM). It also performs on-the-fly error correction of a single dead track based on vertical parity errors (VPE) detected by the tape control-PE module.

The data sync-PE module performs no write data path operations. However, it does a read-after-write during PE write operations.

1.3.2.6 Tape Control-PE Module (M8932) – During a PE read operation, the tape control-PE module operates with the data sync module to detect preamble, data, postamble, and TM. It also checks for vertical parity errors and PE format errors.

During a PE write operation, the tape control-PE module establishes the timing for writing preamble, data, and postamble.

1.3.2.7 Tape Control Common Mode (TCCM) Module (M8933) – The TCCM module contains tape control functions that are used by both PE and NRZI modes. The TCCM module generates clock waveforms used throughout the TM03 from a base clock frequency it receives from the selected slave transport.

When the control register is loaded with a function code requiring tape motion, the function code is decoded by the Massbus interface, and a FWD, REV, or RWND signal is applied to the slave bus. Soon after, a DRIVE SET pulse is generated by the Massbus interface to initialize TM03 circuitry. DRIVE SET pulse enters the TCCM module and produces SLAVE SET PLS and EMD (enable motion delay) – both of which are transmitted to the slave transport via the slave bus. SLAVE SET PLS initiates tape motion. EMD causes a preset to be applied on the read data lines of the slave bus by the slave transport and loads a motion delay counter in the TCCM with the preset. The counter is then upcounted to 2^{14}, at which time ACCL is negated, indicating that the transport is assumed to be up to speed.

A similar motion delay is generated upon termination of a motion command, in which ACCL is asserted, and the TCCM issues STOP, causing the transport to cease tape motion.

During a read operation, read data is multiplexed from the slave bus read data lines through the TCCM module, to the data sync module (for PE) or tape control-NRZI module (for NRZI).

*M9801-YB for 114.3 cm/second (45 inch/second) slaves (TE16).
M8901-YC for 190.5 cm/second (75 inch/second) slaves (TU45).
M8901-YD for 317.5 cm/second (125 inch/second) slaves (TU77).

During a write operation, data is input to the TCCM module from the bit fiddler. The TCCM controls the timing for writing the LRCC and CRCC. It also contains a write multiplexer and write buffer, which:

1. Convert binary characters to PE mode
2. Multiplex 0s and 1s to write PE preambles and postambles
3. Multiplex the generated CRCC onto the write data path
4. Force IDB (identification burst) and TM (tape mark) character patterns onto the write data path.

Data in the TCCM write buffer is output via slave bus drivers on M8937 to the slave, along with REC. REC (record) is derived from WRT CLK, generated in the slave transport; its frequency depends on the mode (PE/NRZI) in which the write operation is performed.

1.4 RELATED DOCUMENTS

Table 1-1 lists documents related to the TM03 formatter.

Table 1-1 Related Documents

Title	Document Number	Description
TE16/TE10W/TE10N DECmagtape Transport Maintenance Manual	EK-TE16-MM-001	Theory and maintenance of TE16, TE10W, and TE10N tape transports
TE16/TE10W/TE10N DECmagtape Transport User Manual	EK-TE16-OP-001	Description, installation and maintenance of the TE16, TE10W, and TE10N tape transports as applicable to a user
TU45A Magnetic Tape Subsystem Maintenance Manual	EK-TU45A-MM-001	Theory and maintenance of TU45A tape transport
TU77 Magnetic Tape Transport Technical Manual, Volume 2	EK-2TU77-TM-001	Theory and maintenance of TU77 tape transport.
TU77 Magnetic Tape Transport User's Guide	EK-TU77-UG-001	Description, installation, and operation of TU77 tape transport.
PDP-11 Peripherals Handbook	-	Provides register descriptions for RH Massbus controllers
H740-D Power Supply Maintenance Manual	DEC-11-H740A-A-D	Theory and maintenance of H740-DA power supply. (The -DA model differs from the -D model by an ac connector used to power the TM03 cooling fan.)

Table 1-1 Related Documents (Cont)

Title	Document Number	Description
RH10 Massbus Controller Maintenance Manual	EK-RH10-MM-002	Theory and maintenance of RH10 Massbus controller
TJU16 Magnetic Tape Subsystem Maintenance Manual	EK-TJU16-MM-002	Theory and maintenance of RH11 Massbus controller
TWU16 Magnetic Tape Subsystem Maintenance Manual	EK-TWU16-MM-PRE	Theory and maintenance of RH70 Massbus controller used with the PDP-11/70
RH20 Massbus Controller Unit Description	EK-RH20-UD-001	Description of RH20 Massbus controller
TM03 Magnetic Tape Formatter User's Manual	EK-TM03-OP-002	Description, installation, and programming information of the TM03.
TM03 Formatter IPB	EK-TM03-IP	Illustrated parts breakdown of TM03.
RH780 Massbus Controller Technical Manual	EK-RH780-TM-001	Theory and maintenance of RH780 Massbus Controller.

1.5 UNIT SPECIFICATIONS

Table 1-2 provides the TM03 unit specifications.

Table 1-2 Unit Specifications

Parameter	Specification
Maximum transfer rate between TM03 and slave	240K bytes/second
Error detection	CRC error detection in forward and reverse read (NRZI) Error correction of single track errors in NRZI and PE Vertical parity error detection throughout TM03
Maximum record length	2^{16} bytes, PE or NRZI
Minimum record length	1 byte, PE; 13 bytes, NRZI (excluding tape mark)
Write lock	Dependent upon write lock signal from slave
Environment	
Operating	10° to 40° C (50° to 104° F) 10 to 90 percent relative humidity Wet bulb: 28° C (82° F) maximum Dew point: 2° C (36° F), minimum

Table 1-2 Unit Specifications (Cont)

Parameter	Specification
Non-operating	-40° to 66° C (-40° to 151° F) 0 to 95 percent relative humidity
Altitude	
Operating	2.4 km (8000 ft), maximum
Non-operating	9.1 km (30,000 ft), maximum
Shock	
Operating	Shall withstand half-sine shock pulse of 10G, peak with 10 ± 3 ms duration
Non-operating	Shall withstand half-sine shock pulse of 40G, peak with 30 ± 10 ms duration, applied perpendicular to each of six surfaces
Vibration	
Operating	Shall withstand vibration of 0.0508 mm (0.002 inch) double amplitude (maximum) in the frequency range of 5 to 50 Hz
Non-operating	Shall withstand vibration of 0.25G peak, in the frequency range of 50 to 500 Hz
Power requirements	
DC	None
AC	90-135/180-270 Vac, 47-63 Hz 0.3 kW
Installation	16.83 cm (6-5/8 inch) panel height 48.3 cm (19 inch) rack mount
Shipping Weight	20.412 kg (45 lb) (uncrated)
Reliability	Established by error rate of slave which is: • Recoverable error rate*: less than one bit in 10^8 reads • Non-recoverable error rate*: less than one bit in 10^9 reads

* A recoverable error is defined as a read error that is recovered within eight successive retries. (Retries on the same spot do not increase the soft error tally; i.e., a read error on block no. 1, record no. 1, that required three retries to recover is recorded as one soft read error.) If the data is not recovered after eight successive retries (nine successive incorrect data transfers), it is counted as one hard error.

CHAPTER 2
PROGRAMMING INFORMATION

Chapter 2 contains programming information required by a user to program a system containing the TM03 formatter. The information provided pertains only to the TM03. Programming information pertaining to other system units can be found in the documentation applicable to these units. Table 1-1 lists the documents available on units that can interface with the TM03.

2.1 REGISTER FUNCTIONS AND FORMATS

The TM03 contains ten registers, some of which have been mentioned in Chapter 1. A summary of the TM03 registers is provided in Table 2-1. Any of the TM03 registers may be read to determine the status of the TM03/transport. Some of the registers may be written, thereby controlling functions and operating parameters.

The TM03 registers are read and written by performing "handshake" operations on the control bus of the Massbus. A register is loaded by the Massbus controller in the following manner.

1. The controller places the select code of the desired TM03 on the drive select lines.
2. The controller places a register select code on the register select lines.
3. It asserts CTOD (controller to drive).
4. It places data on the control lines.
5. The controller then asserts DEM.

The selected TM03 responds to DEM and CTOD asserted by loading the selected register with the data on the control lines. It then asserts TRA. The controller responds by negating DEM, which causes the TM03 to negate TRA; the write operation is thereby terminated.

A TM03 register is read in a similar manner except that CTOD is negated (step 3) and step 4 is eliminated. The selected TM03 responds to DEM asserted and CTOD negated by gating out the contents of the selected register onto the control lines. It then asserts TRA, which, when received by the controller, causes it to strobe in the data on the control lines and negate DEM. The TM03 responds by negating TRA, thereby terminating the operation.

The remainder of Paragraph 2.1 provides a more detailed description of the TM03 registers and their contents. It is primarily for reference, and may be skipped during a first reading.

Table 2-1 TM03 Registers

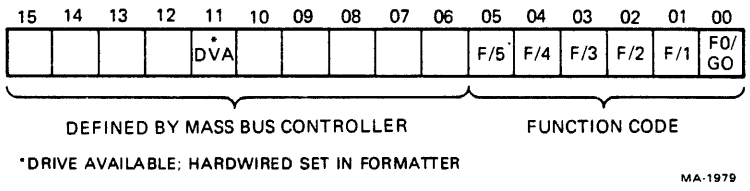
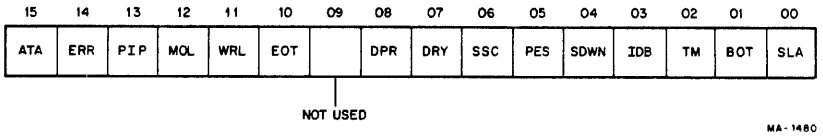
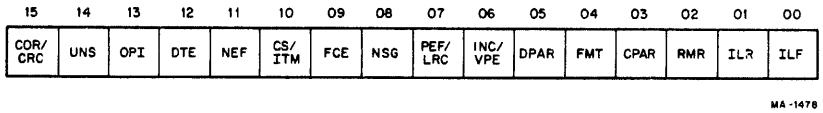
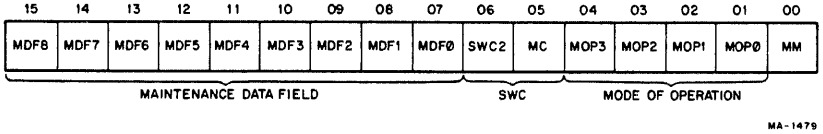
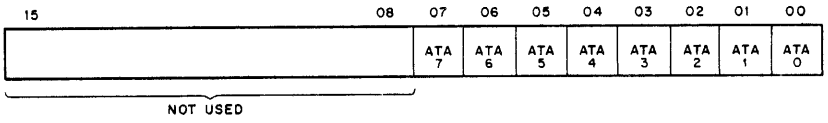
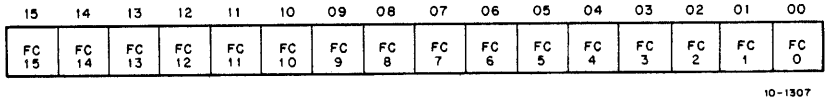
Address Code (Octal)	Name	Type	Description
00	Control 1 (CS1)	Read/write	Contains the function code including the GO bit. 
01	Status (DS)	Read only	Contains all nonerror status information plus the error summary bit. 
02	Error (ER)	Read only	Contains all error indications. 
03	Maintenance (MR)	Read/write	Controls diagnostic functions. 

Table 2-1 TM03 Registers (Cont)

Address Code (Octal)	Name	Type	Description
04	Attention Summary (AS)	Read/write	Indicates the attention active status of each TM03 (one bit/TM03).
05	Frame Count (FC)	Read/write	For a write data transfer operation, contains the 2's complement of the number of tape characters to be transferred. For a space operation, contains the 2's complement of the number of records to be spaced. For a read data transfer operation, contains the 2's complement of the number of characters read.
06	Drive Type (DT)	Read only	Indicates the type of formatter and the type and status of the transport (e.g., existing formatter and transport with power applied).





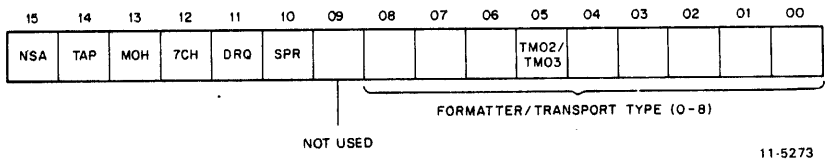
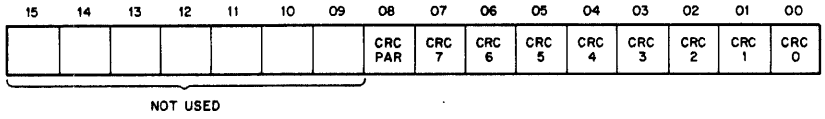
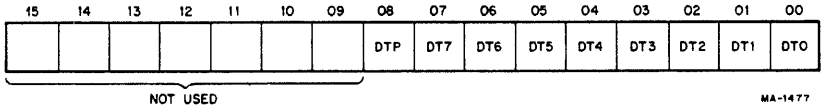
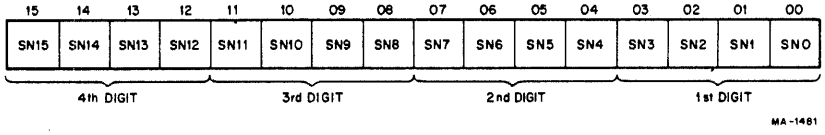
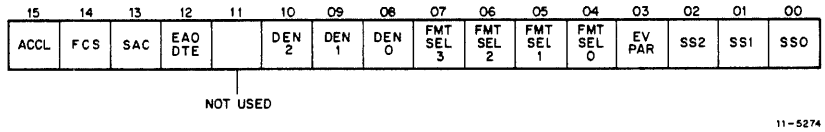


Table 2-1 TM03 Registers (Cont)

Address Code (Octal)	Name	Type	Description
07	Check Character (CK)	Read only	For an NRZI operation, contains the CRC error character.  For a PE operation, contains the dead-track indications. 
10	Serial Number (SN)	Read only	Contains the last four digits of the transport serial number. 
11	Tape Control (TC)	Read/write	Contains the transport selection and configuration codes. 

2.1.1 Control Register [(CS1) Register 00_8]

The control register is a read/write register (Figure 2-1) which receives operational commands from the Massbus controller via the control bus. This register operates in conjunction with the tape control register to control the operation of the selected transport.

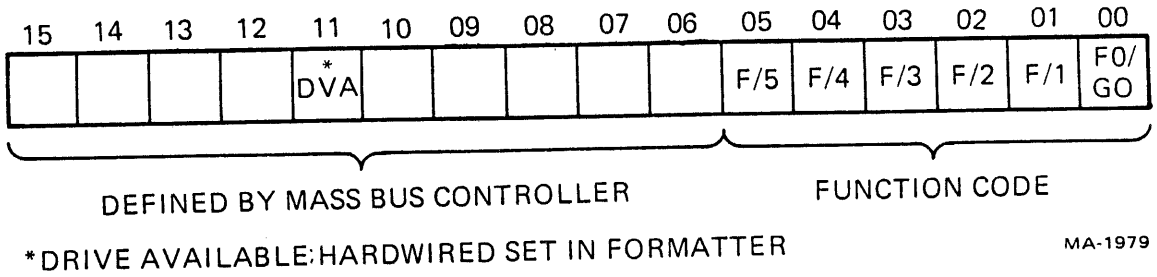


Figure 2-1 Control Register Format

The control register is shared with the Massbus controller. Bits 00 through 05 and bit 11 are located in the TM03. The remaining nine bits are located in the controller.

The TM03/transport responds to the 14 function codes listed in Table 2-2. If the control register is loaded with a function code (with GO bit set) that does not agree with those listed in the table, an illegal function error (ILF) is generated. Thus, an ILF is generated for codes 05_8, 13_8, 15_8, 17_8, 23_8, 35_8, etc., but not for 00_8, 02_8, 04_8, 06_8, 10_8, 12_8, etc.

Table 2-2 Command Function Codes

Function Code F(0–5) (Octal)	Operation	Description
01	No Op	Performs no operation. Clears GO bit in control register.
03	Rewind Off-Line*	1. Initiates a rewind on selected transport and places it off-line. 2. Clears GO bit. 3. Sets the following bits in the status register: Drive Ready (DRY) Slave Status Change (SSC) Attention Active (ATA)
07	Rewind	1. Initiates a rewind to BOT marker on selected transport and clears the GO bit. 2. Sets DRY, PIP, and ATA bits in the status register during rewind. 3. When BOT is sensed, sets SSC and clears PIP.

*Requires manual intervention to return transport on-line.

Table 2-2 Command Function Codes (Cont)

Function Code F(0–5) (Octal)	Operation	Description
11	Drive Clear	Similar to initialize. Resets all TM03 and selected transport logic. Does not affect unselected transports.
21	Read-In Preset	Presets the tape control register (R11) to select slave 0, odd parity, PDP-10 core dump format, and 800 bits/inch NRZI; then causes slave 0 to rewind.
25	Erase	Erases approximately 7.6 cm (3 inches) of tape. Clears GO bit and sets ATA on termination.
27	Write Tape Mark	Writes a special tape record on the selected transport. Clears GO bit and sets ATA bit on termination.
31	Space Forward	Moves tape forward (toward EOT) on the selected transport over the number of records specified by the frame count register. Aborts space operation if TM or EOT is detected prior to specified frame count. Clears GO bit and sets ATA on termination.
33	Space Reverse	Moves tape in reverse (toward BOT) on the selected transport over the number of records specified by the frame count register. Aborts space operation if TM or BOT is detected prior to specified frame count. Clears GO bit and sets ATA on termination.
51	Write Check Forward	Same as Read Forward.
57	Write Check Reverse	Same as Read Reverse.
61	Write Forward	Writes forward one tape record on the selected transport. Record length is determined by frame count register. Clears GO bit on command termination.

Table 2-2 Command Function Codes (Cont)

Function Code F(0–5) (Octal)	Operation	Description
71	Read Forward	Reads forward one tape record on the selected transport. Clears GO bit on command termination.
77	Read Reverse	Reads reverse one tape record on the selected transport. Clears GO bit on command termination.

2.1.2 Status Register [(DS) Register 01_8]

The status register is a 16-bit, read-only register that stores the tape system status information. Figure 2-2 illustrates the status register format and Table 2-3 defines the bit positions. Although the status register multiplexer is located in the TM03, inputs to this multiplexer may be generated either by a selected transport, any transport, or the TM03 logic itself. Because of this fact, each bit position in Table 2-3 is identified by one or more of the following designators to indicate the origin of the input signal.

(SS) = Selected transport
(S) = Any transport
(M) = TM03 logic

Table 2-3 Status Register Bit Positions

Bit Position	Name	Description
00 (SS)	Slave Attention (SLA)	Indicates that a selected transport has come on-line.
01 (SS)	Beginning of Tape (BOT)	Indicates that a selected transport has detected the BOT marker.
02 (M)	Tape Mark (TM)	Indicates that a tape mark has been detected. Remains asserted until the next tape motion is initiated.
03 (M)	Identification Burst (IDB)	Indicates that a phase-encoded (PE) identification burst has been detected. Asserted until a subsequent tape motion command is initiated.
04 (SS)	Settle Down (SDWN)	Indicates that tape motion on the selected transport is stopping.

Table 2-3 Status Register Bit Positions (Cont)

Bit Position	Name	Description
05 (SS)	Phase-Encoded Status (PES)	Indicates that the selected transport is configured for PE operation. Is negated during NRZI operation.
06 (S)	Slave Status Change (SSC)	Indicates that any transport has just gone on-line or off-line, or has completed a rewind operation.
07 (M)	Drive Ready (DRY)	Indicates that both the TM03 and the selected transport are ready to accept a command.
08 (M)	Drive Present (DPR)	Hard-wired set.
09	Not used	
10 (SS)	End of Tape (EOT)	Indicates that the selected transport has detected the EOT marker during forward tape motion. Is negated when the EOT marker is detected during reverse tape motion.
11 (SS)	Write Lock (WRL)	Indicates that the selected transport is write protected.
12 (SS)	Medium On-Line (MOL)	Indicates that the selected transport has tape loaded and is on-line.
13 (M/SS)	Positioning in Progress (PIP)	Indicates that the selected transport is performing a tape motion operation. This bit is asserted by the TM03 (M) during a space or by the selected transport (SS) during a rewind.
14 (M)	Composite Error (ERR)	Indicates that an error condition has occurred. Is asserted whenever any bit in the error register is set.
15 (M)	Attention Active (ATA)	Is asserted whenever the ATTN interface signal is generated. Indicates one of the following: 1. The TM03 and the selected transport require servicing. 2. The TM03 and the selected transport have become ready after a nontransfer operation. 3. A transport status change has occurred.

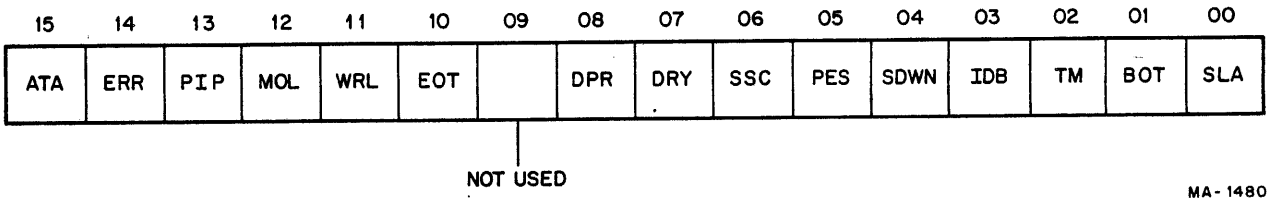


Figure 2-2 Status Register Format

2.1.3 Error Register [(ER) Register 02_8]

There are 16 different error conditions that can be detected in the TM03/transport system. The error register is a 16-bit, read-only register that stores all of the tape system error indications.

TM03/transport errors are categorized as Class A and Class B. A Class B error will terminate an in-progress data transfer; a Class A error will not. However, the Massbus controller is notified of any error during a data transfer by the immediate assertion of exception (EXC) on the Massbus. If the TM03/transport is not performing any operation, or is performing a rewind (i.e., the GO bit is clear), the controller is immediately notified of an error condition by the assertion of ATTN on the Massbus.

Figure 2-3 illustrates the error register format and Table 2-4 lists the error bit indicators.

Table 2-4 Error Register Bit Indicators

Bit Position	Name	Description	Type
00	Illegal Function (ILF)	Indicates that an illegal function code has been transmitted.	Class B
01	Illegal Register (ILR)	Indicates that a read or write from a nonexistent register is attempted.	Class A
02	Register Modification Refuse (RMR)	Indicates that during a transport operation (GO = 1), a write into one of the registers is attempted. (Does not apply for the maintenance or attention summary registers.)	Class A
03	Control Bus Parity (CPAR)	Indicates that incorrect control bus parity is detected.	Class A
04	Format (FMT)	Indicates that a data transfer with an incorrect format code is attempted. When the M8915 bit fiddler is used, a FMT error could also indicate: 1. Microcode parity error 2. M8915 data parity error 3. Illegal microcode instruction	Class B
05	Data Bus Parity Error (DPAR)	Indicates that incorrect data bus parity has occurred.	Class A
06	Incorrectable Data Error or Vertical Parity Error (INC/VPE)	During a PE read operation, indicates that one of the following has occurred: 1. Multiple dead tracks 2. Dead tracks without parity errors 3. Parity errors without dead tracks 4. Skew overflow 5. Parity error in bit fiddler.	Class A

Table 2-4 Error Register Bit Indicators (Cont)

Bit Position	Name	Description	Type
		During an NRZI read operation, indicates that a vertical parity error has occurred or that data has occurred after the skew delay is over.	
07	Format Error or LRC Error (PEF/LRC)	During a PE read operation, indicates than an incorrect preamble or postamble is detected. During an NRZI write operation, indicates that the LRCC read off the tape does not match the LRCC computed from the characters read off the tape.	Class A
08	Nonstandard Gap (NSG)	Indicates that a tape character is detected during the first half of the end-of-record gap while a write operation is in progress. Never set during a read operation.	Class A
09	Frame Count Error (FCE)	Indicates that a space operation has terminated and the frame counter is not cleared. Also asserted when the Massbus controller fails to negate RUN when the TM03 asserts EBL.	Class A
10	Correctable Skew or Illegal Tape Mark (CS/ITM)	During a PE read operation, indicates that excessive but correctable skew is detected. (This condition is only a warning and does not indicate bad data.) During an NRZI read, indicates that characters not legally a tape mark have been read and recognized as a tape mark (e.g., such as a record less than the 10-character minimum).	Class A
11	Nonexecutable Function (NEF)	Indicates one of the following: 1. A write operation is attempted on a write-protected transport. 2. A space reverse, read reverse, or write check reverse is attempted when the tape is at BOT. 3. The DEN2 bit in the tape control register does not agree with the PES status bit during a write operation. 4. A space or write operation is attempted when FCS = 0 in the tape control register.	Class B

Table 2-4 Error Register Bit Indicators (Cont)

Bit Position	Name	Description	Type
		5. A write operation is attempted with DEN2 = 0 in the tape control register (NRZI mode) and the 2's complement of a number less than 13_8 is in the frame count register. 6. The type of phase-locked loop modules (M8901-YB, YC, or YD) do not agree with the type of transport as specified by the drive type register. This indicates that the TM03 and the transport are not operating at the same tape speed.	
12	Drive Timing Error (DTE)	Indicates one of the following: 1. During a write operation, WCLK was not received from the Massbus controller in time to provide a valid tape character. 2. A data transfer (read/write) was attempted when the data bus of the Massbus was already occupied.	Class B
13	Operation Incomplete (OPI)	During a read/write or space operation, indicates that an end of record has not been detected within 7 seconds from command initiation. Also set during a read reverse or a space reverse if BOT is detected.	Class B
14	Unsafe (UNS)	Indicates one of the following: 1. A program-controlled operation is attempted on a selected transport that is not on-line. 2. An imminent power failure is detected (AC LO).	Class B
15	Correctable Data Error or CRC Error (COR/CRC)	During a PE read operation, indicates that a single dead track has occurred. During an NRZI operation, indicates that the CRCC read off the tape does not match the CRCC computed from the data read off the tape.	Class A

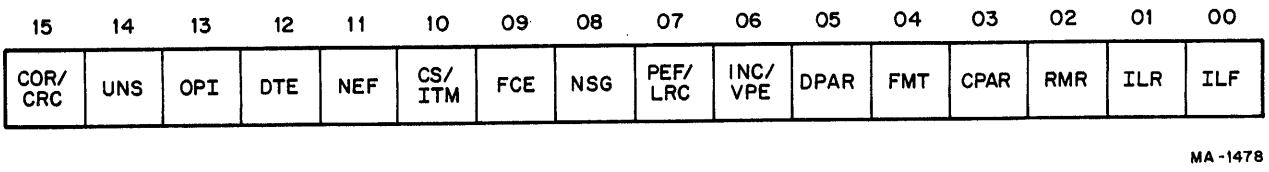


Figure 2-3 Error Register Format

2.1.4 Maintenance Register [(MR) Register 03_8]

The maintenance register (M8905-YB) is a 16-bit, read/write register (Figure 2-4) that allows complete diagnostic testing of the TM03 data paths and error detection circuitry. The maintenance register can configure the data paths into five wraparound loops, each loop testing certain TM03 circuits. The maintenance register data field is part of these loops, and is used to read or write test data into the TM03. Table 2-5 briefly describes the bits of the maintenance register.

Table 2-5 Maintenance Register Bit Positions

Bit Position	Name	Description
00	Maintenance Mode (MM)	When set, configures the TM03 for maintenance mode operation.
01–04	Maintenance Operation Code (MOP0–3)	Controls command execution during the maintenance mode. (MM and MOP function together to alter normal command execution during maintenance mode operation.)
05	Maintenance Clock (MC)	Controls data sequencing through the TM03 data path in maintenance mode.
06	Tape Speed Clock (SWC2)	A clock signal generated by the selected slave. Frequency depends on the tape speed of the selected slave. Used to monitor maintenance mode read operations.
07–15	Maintenance Data Field (MDF0–8)	Buffers the data generated during wraparound operations. At the end of normal NRZI transfers, contains the LRC of the last record.

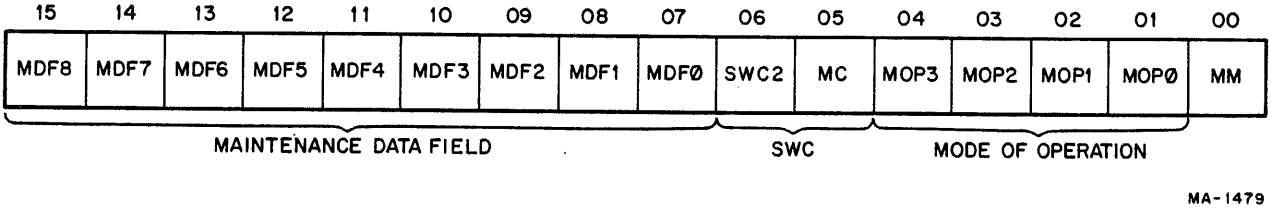


Figure 2-4 Maintenance Register Format

2.1.5 Attention Summary Register [(AS) Register 04_8]

The attention summary register (M8909-YA) is a read/write "pseudo-register" that consists of from one to eight bits, depending on the number of drives (TM03s) on the Massbus. The term "pseudo-register" refers to the fact that only one register bit position is physically contained in each TM03. This bit position reflects the state of the ATA status bit for that TM03. Hence, bit position 0 of the attention summary register is generated by the ATA bit of TM03 No. 0; bit position 1 is generated by the ATA bit of TM03 No. 1, and so on to bit 7. Bits 8 through 15 are not used.

Unlike the other TM03 registers, the attention summary register is directly selected by the controller without first addressing a particular TM03. Thus, for a single attention summary register read operation, every TM03 in the system responds by placing the state of its ATA bit in the appropriate bit position on the control bus and disabling its remaining 15 control bus transmitters. This control bus configuration appears as a single register output which collectively informs the controller of all TM03s that require attention (i.e., ATA = 1). The controller can then selectively examine the error or status registers of each of the affected TM03s to determine the cause of the individual attention conditions.

The controller can also write into the attention summary register; however, the significance of the bits being written is unusual. Writing a 1 into a bit position resets the ATA bit in the TM03 assigned to that bit position; however, writing a 0 has no effect. This unique writing scheme allows the controller to reset, after inspection, all summary bits that were set, without accidentally resetting those bits that may have become set in the meantime. The following table illustrates the effects of writing into an attention summary bit position.

ATA Bit Before	Summary Bit Written	ATA Bit After
0	0	0
1	0	1
0	1	0
1	1	0

2.1.6 Frame Count Register [(FC) Register 05_8]

The frame count register (M8909-YA) is a 16-bit, read/write register that counts tape events. During a data transfer operation (read/write), this register is incremented each time a tape character is transferred to or from the tape. However, during a space operation, this register is incremented each time a record is detected. The register output may be read by the controller at any time, but the controller can only write into this register when the transport is not performing a space operation or data transfer (GO negated).

For a write operation, the frame count register is loaded, prior to write initiation, with the 2's complement of the number of tape characters to be written. During the writing process, the frame count register is incremented each time a tape character is recorded. Normal write data transfer termination is accomplished when the frame count register overflows to zero. For a space operation, the frame count register functions similarly to a write, except it is loaded with the 2's complement of the number of records to be spaced and is then incremented each time a record is detected. Space termination is accomplished when the register overflows to zero. For a read operation, this register is automatically reset prior to read initiation. The register is then incremented each time a tape character is read. Thus, at the end of the read operation, the frame count register contains a count of the number of characters read.

2.1.7 Drive Type Register [(DT) Register 06_8]

The drive type register (M8933) is a 16-bit, read-only register, the content of which identifies the particular type of formatter and transport being used. When a read from the drive type register is performed, the register output is applied to the appropriate multiplexer bit positions. Bits 0 through 8 (DT0–8) of the drive type register identify the type and status of the selected formatter and transport. If a nonexistent transport is selected or if the selected transport is not powered up, DT0–8 will contain 050_8. If the selected transport is powered up, the drive type code will be $05X_8$, where X represents bits DT0, DT1, and DT2 and indicates the type of slave. Bits DT0 through DT8 are coded as shown below for the TM03. Neither INIT nor drive clear can affect bits DT0–8.

DT8	DT7	DT6	DT5*	DT4	DT3	DT2	DT1	DT0	
0	0	0	1	0	1	0	0	0	= Unselected slave
0	0	0	1	0	1	0	0	1	= 114.3 cm/second (45 in/s), slave selected
0	0	0	1	0	1	0	1	0	= 190.5 cm/second (75 in/s), slave selected
0	0	0	1	0	1	1	0	0	= 317.5 cm/second (125 in/s), slave selected

Figure 2-5 illustrates the drive type register format and Table 2-6 briefly describes each bit position.

Table 2-6 Drive Type Register Bit Positions

Bit Position	Name	Description
00–08	Drive Type (DT0–8)	Specifies the type of formatter and transport.
09	-	Spare bit.
10	Slave Present (SPR)	Asserted when a transport is powered up and has been assigned the selection code contained in the tape control register.
11	Drive Request Required (DRQ)	Always negated to indicate that the device is a single-port unit.
12	7-Channel (7CH)	Always negated. The TM03 does not interface with 7-channel transports.
13	Moving Head (MOH)	Always negated to indicate that the device is not a moving head unit.
14	Tape Drive (TAP)	Always asserted to indicate that the device is a tape transport.
15	Not Sector Addressed (NSA)	Always asserted to indicate that the device is not sector addressable.

*DT5 will indicate the type of formatter being used.
DT5 = 0 = TM02
DT5 = 1 = TM03

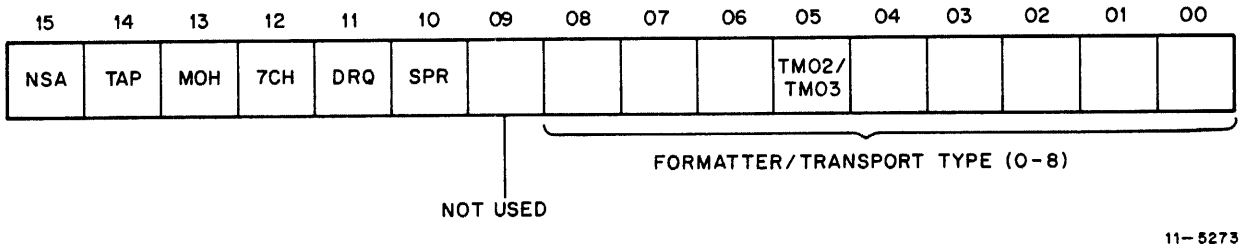


Figure 2-5 Drive Type Register Format

2.1.8 Check Character Register [(CK) Register 07_8]

The check character register (M8905-YB) is a 9-bit, read-only register that permits the programmer to check the validity of a data transfer. At the end of an NRZI read operation, this register contains the CRCC for that operation. Hence, the programmer can determine if the CRCC generator logic is functioning properly. At the end of a PE read operation, however, this register contains a dead track indication (DT = 1) of any track that may have dropped one or more bits during the operation.

Figure 2-6 illustrates the check character register format for both NRZI and PE modes.

2.1.9 Serial Number Register [(SN) Register 10_8]

The serial number register is a 16-bit, read-only register that contains a BCD representation of the 4 least-significant digits of the transport serial number.

Figure 2-7 illustrates the serial number register format.

2.1.10 Tape Control Register [(TC) Register 11_8]

The tape control register (M8905-YB) is a 16-bit, read/write register that selects an existing transport and configures it to a particular operational mode.

Figure 2-8 illustrates the tape control register and Table 2-7 briefly describes each bit position.

Table 2-7 Tape Control Register Bit Positions

Bit Position	Name	Description
00–02	Slave Select (SS0–2)	Specifies the unit number of the transport to be used.
03	Even Parity (EV PAR)	When set for NRZI operation, even parity is written or read from tape. Ignored during PE operation. (PE operations are always odd parity.)
04–07	Format Select (FMT SEL0–3)	Specifies Massbus-to-tape character formatting during a write operation, or tape character-to-Massbus formatting during a read operation. Format codes are as follows.* 0000–PDP-10 Format: "10-Core Dump" 0001–PDP-15 Format: "15-Core Dump" 0011–PDP-10 Format: "10-Compatible" 1100–PDP-11 Format: "11-Normal" 1101–PDP-11 Format: "11-Core Dump" 1110–PDP-15 Format: "15-Normal" 1111–PDP-11 Format: Reserved

Table 2-7 Tape Control Register Bit Positions(Cont)

Bit Position	Name	Description
08–10	Density Select (DEN0–2)	Specifies the tape character density during read or write operations as follows.† DEN2 DEN1 DEN0 Density (bits/inch) 0 1 1 800 NRZI 1 0 0 1600 PE 1 0 1 Reserved 1 1 0 Reserved 1 1 1 Reserved
11	Not used	
12	Enable Abort on Data Transfer Errors (EAODTE)	When set, immediately aborts a write or read operation for one of the following errors. 1. COR/CRC – Error register bit 15. 2. PEF/LRC – Error register bit 7. 3. INC/VPE – Error register bit 6. 4. DPAR – Error register bit 5.
13	Slave Address Change (SAC)	Asserts whenever the slave select bits of the TC register are changed. Negates on the next drive set pulse.
14	Frame Count Status (FCS)	Is normally set at the end of a write into the frame count register. However, if FCS = 0, and a space or write command with GO = 1 is loaded, a nonexecutable function (NEF) error is generated and the command is not executed. Is reset when frame count register overflows.
15	Acceleration (ACCL)	This read-only bit is asserted when the transport is not actively reading or writing data.

* 1. Codes 0000 and 0011 use an M8915 data formatting module.

2. Codes 1100 and 1110 use an M8906 data formatting module.

3. All other format codes are invalid. An invalid code causes a format error (FMT – error register bit 4) when a data transfer command with GO = 1 is loaded.

†DEN2 bit selects 800 or 1600 bits/in. DEN1 and DEN0 bits are not used. DEN codes 5_8, 6_8, and 7_8 are reserved for future use.

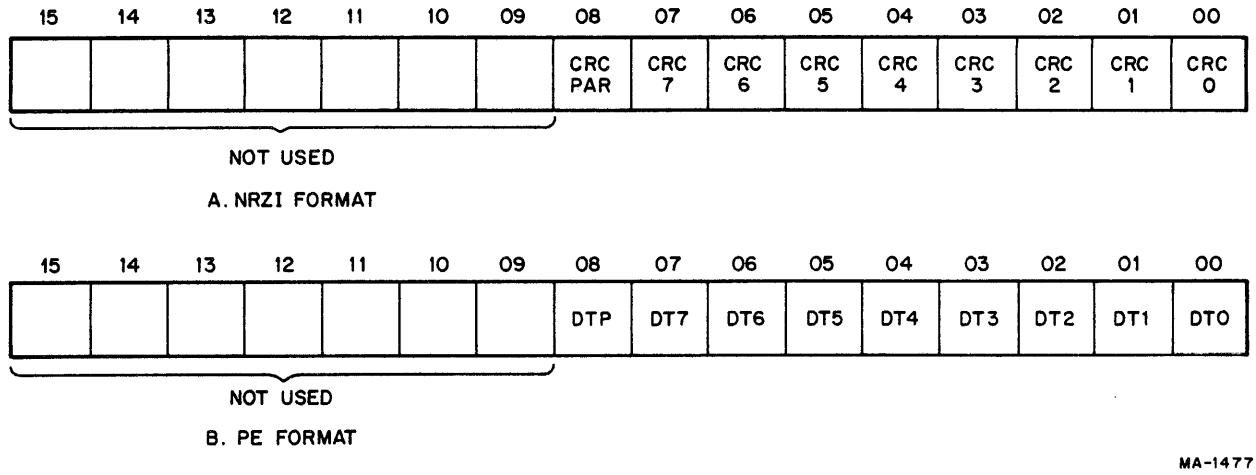


Figure 2-6 Check Character Register Format

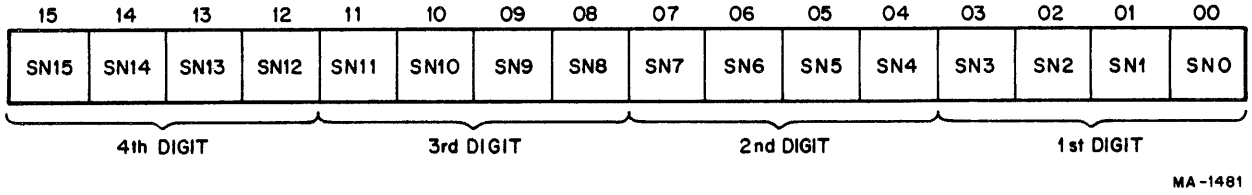


Figure 2-7 Serial Number Register Format

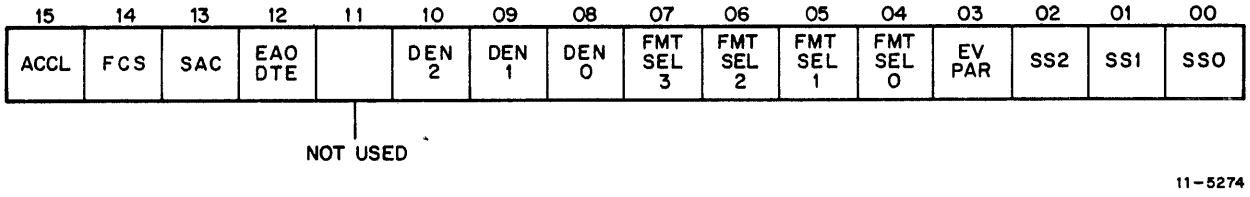


Figure 2-8 Tape Control Register Format

2.2 DATA FORMATS

This section illustrates how the TM03 maps Massbus transfers onto tape during write operations and how tape characters are mapped onto the Massbus data lines during read operations. PDP-10, PDP-11, and PDP-15 processor bits are defined and the location of these bits during a Massbus transfer is shown. The pack/unpack format of the processor words into tape frames is shown for the various formatting modes.

2.2.1 Massbus/TM03 Transfers

Consider a single record that is to be read from or written on tape. Assume four Massbus transfers will occur during the writing (reading) of this record and that the contents of the first transfer will be 111111_8, the contents of the second transfer will be 222222_8, the third 333333_8, and the fourth 444444_8. If the write (or read) is in a forward direction, the four Massbus/TM03 transfers will be:

111111_8 - First transfer
222222_8 - Second transfer
333333_8 - Third transfer
444444_8 - Fourth transfer.

If the read is in a reverse direction, the four Massbus/TM03 transfers will be:

444444_8 - First transfer
333333_8 - Second transfer
222222_8 - Third transfer
111111_8 - Fourth transfer.

Words transferred between memory and the TM03 are formatted on the Massbus according to which processor is used. Two transfers are required to transmit a 36-bit PDP-10 word while only a single transfer is required for a 16-bit PDP-11 word or an 18-bit PDP-15 word. The word formats on the Massbus for the PDP-10, PDP-11, and PDP-15 are shown in Tables 2-8, 2-9 and 2-10. The 18 data lines on the Massbus are designated D0–D17.

Table 2-8 PDP-10 Massbus Word Format

D17–D0	Massbus Data Lines
B0–B17	First Massbus Transfer*
B18–B35	Second Massbus Transfer*

B0 = MSB; B35 = LSB

* In read reverse, the order of Massbus transfers are reversed; i.e., B18–B35 = first transfer and B0–B17 = second transfer.

Table 2-9 PDP-11 Massbus Word Format

D17	D16	D15–D0	Massbus Data Lines
		R15–R0	Massbus Transfer

R0 = LSB; R15 = MSB

Table 2-10 PDP-15 Massbus Word Format

D17–D0	Massbus Data Lines
N0–N17	Massbus Transfer

N0 = MSB; N17 = LSB

2.2.2 TM03/Tape Frame Packing

In a write operation, the processor data word in the TM03 is disassembled and packed onto tape in a number of tape characters or frames. The number of frames depends on the processor used and the mode of operation. In a read operation, the tape frames are read off tape (unpacked) and assembled into a data word for Massbus transfer. The packing/unpacking formats are shown in Tables 2-11 through 2-16 for the PDP-10, PDP-11, and PDP-15 processors in various format modes. During a read-reverse operation, the frames are read off tape in reverse order.

Table 2-11 PDP-10 Compatability Mode – Format Code 0011

Tape Frames	Tape Track Positions								
	TP	T7 (MSB)	T6	T5	T4	T3	T2	T1	T0 (LSB)
1	P	B0	B1	B2	B3	B4	B5	B6	B7
2	P	B8	B9	B10	B11	B12	B13	B14	B15
3	P	B16	B17	B18	B19	B20	B21	B22	B23
4	P	B24	B25	B26	B27	B28	B29	B30	B31

Table 2-12 PDP-10 Core Dump Mode – Format Code 0000

Tape Frames	Tape Track Positions								
	TP	T7 (MSB)	T6	T5	T4	T3	T2	T1	T0 (LSB)
1	P	B0	B1	B2	B3	B4	B5	B6	B7
2	P	B8	B9	B10	B11	B12	B13	B14	B15
3	P	B16	B17	B18	B19	B20	B21	B22	B23
4	P	B24	B25	B26	B27	B28	B29	B30	B31
5	P	Ø	Ø	Ø	Ø	B32	B33	B34	B35

Table 2-13 PDP-11 Normal Mode - Format Code 1100

Tape Frames	Tape Track Positions								
	TP	T7 (MSB)	T6	T5	T4	T3	T2	T1	T0 (LSB)
1	P	R7	R6	R5	R4	R3	R2	R1	R0
2	P	R15	R14	R13	R12	R11	R10	R9	R8

Table 2-14 PDP-11 Core Dump Mode - Format Code 1101

Tape Frames	Tape Track Positions								
	TP	T7	T6	T5	T4	T3 (MSB)	T2	T1	T0 (LSB)
1	P	0	0	0	0	R3	R2	R1	R0
2	P	0	0	0	0	R7	R6	R5	R4
3	P	0	0	0	0	R11	R10	R9	R8
4	P	0	0	0	0	R15	R14	R13	R12

Table 2-15 PDP-15 Normal Mode - Format Code 1110

Tape Frames	Tape Track Positions								
	TP	T7 (MSB)	T6	T5	T4	T3	T2	T1	T0 (LSB)
1	P	N2	N3	N4	N5	N6	N7	N8	N9
2	P	N10	N11	N12	N13	N14	N15	N16	N17

Table 2-16 PDP-15 Core Dump Mode - Format Code 0001

Tape Frames	Tape Track Positions								
	TP	T7	T6	T5 (MSB)	T4	T3	T2	T1	T0 (LSB)
1	P	0	0	N0	N1	N2	N3	N4	N5
2	P	0	0	N6	N7	N8	N9	N10	N11
3	P	0	0	N12	N13	N14	N15	N16	N17

It is important to note that in any given transfer, the frame count register must contain the 2's complement of the number of frames required to transfer complete processor words to or from tape. For example, in the PDP-10 core dump mode shown in Table 2-12, it takes five tape frames to read or write a word on tape. The frame count register must be loaded with the 2's complement of 5 times the number of words read or written; e.g.,

A 25-word transfer = 25 × 5 = 125 tape frames
A 26-word transfer = 26 × 5 = 130 tape frames
A 27-word transfer = 27 × 5 = 135 tape frames.

2.3 COMMAND FUNCTIONS

There are 14 commands implemented by a TM03/transport system. The commands are listed and briefly described in Table 2-17. Function codes not listed in Table 2-17 are treated as illegal functions. Commands, other than drive clear, will be executed only if they are directed to an on-line transport.

Paragraphs 2.3.1 through 2.3.12 provide additional information about the command functions.

Table 2-17 Command Functions

Function Code F (0–5) (Octal)	Operation	Description
01	No Op	Performs no operation. Clears GO bit in control register.
03	Rewind Off-Line*	1. Initiates a rewind on selected transport and places it off-line. 2. Clears GO bit. 3. Sets the following bits in the status register: Drive Ready (DRY) Slave Status Change (SSC) Attention Active (ATA)
07	Rewind	1. Initiates a rewind to BOT marker on selected transport and clears the GO bit. 2. Sets DRY, PIP, and ATA bits in the status register during rewind. 3. When BOT is sensed, sets SSC and clears PIP.
11	Drive Clear	Similar to initialize. Resets all TM03 and selected transport logic. Does not affect unselected transports.

*Requires manual intervention to return transport on-line.

Table 2-17 Command Functions (Cont)

Function Code F (0–5) (Octal)	Operation	Description
21	Read-In Preset	Presets the tape control register (R11) to select slave 0, odd parity, PDP-10 core dump format, and 800 bit/inch NRZI; then causes slave 0 to rewind.
25	Erase	Erases approximately 7.6 cm (3 inches) of tape. Clears GO bit and sets ATA on termination.
27	Write Tape Mark	Writes a special tape record on the selected transport. Clears GO bit and sets ATA bit on termination.
31	Space Forward	Moves tape forward (toward EOT) on the selected transport over the number of records specified by the frame count register. Aborts space operation if TM or EOT is detected prior to specified frame count. Clears GO bit and sets ATA on termination.
33	Space Reverse	Moves tape in reverse (toward BOT) on the selected transport over the number of records specified by the frame count register. Aborts space operation if TM or BOT is detected prior to specified frame count. Clears GO bit and sets ATA on termination.
51	Write Check Forward	Same as read forward.
57	Write Check Reverse	Same as read reverse.
61	Write Forward	Writes forward one tape record on the selected transport. Record length is determined by frame count register. Clears GO bit on command termination.
71	Read Forward	Reads forward one tape record on the selected transport. Clears GO bit on command termination.
77	Read Reverse	Reads reverse one tape record on the selected transport. Clears GO bit on command termination.

2.3.1 No-Op

This command causes immediate reset of the GO bit and assertion of DRY. No tape motion or status change occurs in the selected slave. No attention is generated.

2.3.2 Rewind, Off-Line

The selected slave begins rewinding and goes off-line. GO is reset and DRY, SSC, and ATA become asserted (SSC becomes asserted because the slave has gone off-line).

Operator intervention is required to bring the slave back on-line.

NOTE

This command generates only one attention, whereas a rewind command may generate either one or two attentions.

2.3.3 Rewind

The selected slave executes a rewind back to the reflective strip marking beginning of tape (BOT). Sequencing of a rewind command proceeds as follows.

1.0 When a rewind command is loaded with GO = 1, the TM03 first checks the settle-down (SDWN) bit in the status register.

   a. If SDWN = 0, the selected slave immediately begins rewinding.

   b. If SDWN = 1 (indicating that the selected slave is slowing to a halt after completion of a prior command) and the last command executed called for tape motion in the reverse direction, the selected slave immediately begins rewinding.

   c. If SDWN = 1 and the last command executed called for tape motion in the forward direction, the TM03 delays execution of the rewind until SDWN = 0, indicating that the selected slave has stopped.

2. As soon as the slave has recognized the rewind command, the TM03 returns to the ready state and DRY and ATA become asserted. In steps 1a and b above, the time from initiation of the control bus write sequence which loads the rewind command, until reassertion of DRY is 2 μs. In step 1c above, reassertion of DRY may not occur for up to 15 ms after initiation of the rewind sequence.

3. Once the selected slave reaches BOT, it will cause slave status change (SSC) and ATA to become asserted. If selected slave was already at BOT when the rewind command was loaded, the ATA condition generated in step 2 above and the ATA condition generated in this step will occur together.

4. The following examples will indicate the states of important status bits during a rewind sequence. (The possibility of SLA and SSC becoming asserted due to status changes in slaves other than the rewinding slave will not be treated.)

   a. During the time between reception of the rewind command and initiation of a rewind by the selected slave: DRY = 0, ATA = 0, SSC = 0, SLA = 0, SDWN = 0 or 1, PIP = 0

   b. After initiation of the rewind, if the selected slave was already at BOT: DRY = 1, ATA = 1, SSC = 1, SLA = 0, SDWN = 0, PIP = 0, BOT = 1

c. After initiation of the rewind, if the selected slave was not at BOT: DRY = 1, ATA = 1, SSC = 0, SLA = 0, PIP = 1

d. After completion of the rewind, if the selected slave was not already at BOT: DRY = 1, ATA = 1, SLA = 0, SSC = 1, SDWN = 0, PIP = 0, BOT = 1 (identical to case in step 4b above)

Note that SSC is an indication of status changes in at least one slave. Thus, it should not be cleared until all slaves have been polled to confirm their status.

5. In a multi-slave system, the presence of rewinding slaves on the TM03 slave bus does not interfere with the execution of commands by selected slaves that are not rewinding. Any command recognized as a legal function by the TM03 may be issued to a rewinding slave if DRY = 1. If this is done, the following sequence of events will occur.

   a. When command is loaded, GO becomes asserted.

   b. Execution of command is deferred until rewind is complete (until PIP becomes negated); GO remains asserted.

   c. When rewind reaches completion, PIP becomes negated and SSC becomes asserted; command execution is initiated.

   d. When command reaches completion, ATA becomes asserted because of prior assertion of SSC.

2.3.4 Drive Clear

This command performs a reset on the TM03 and selected slave but does not affect unselected slaves. Unlike any other command, drive clear can be executed on the TM03/transport even if MOL = 0.

2.3.4.1 Drive Clear Resets – A drive clear command resets SLA in the selected slave, SSC if no other slaves have current attention-demanding conditions, TM, IDB, ERR, and ATA in the status register. The drive clear command also resets all but bit 6 of the maintenance register, FCS in the tape control register, all bits in the error register except bit 14 (UNS), and UNS if the TM03 is not experiencing a power-fail.

The time from reception of a drive clear command to reassertion of DRY is 2 μs. If drive clear is issued to a TM03 that is experiencing a power-fail, ATA and ERR will become asserted when DRY becomes asserted. Drive clear cannot affect a rewinding slave.

2.3.4.2 Drive Clear versus Initialize (INIT) – INIT differs from drive clear in the following aspects.

1. INIT may be issued at any time.
2. INIT affects all slaves, not just the selected slave.
3. INIT will abort any NRZI error correction cycle that may be in progress.

INIT resets GO in the control register; SLA (all slaves), SSC, TM, IDB, ERR, and ATA in the status register; all but bit 6 of the maintenance register; FCS in the tape control register; and all bits in the error register except bit 14 (UNS) and UNS if the TM03 is not experiencing a power-fail. INIT sets DRY. INIT will also clear all NRZI error correction cycles. INIT, like drive clear, requires 2 μs for completion. If the TM03 is experiencing a power-fail when INIT is issued, ATA and ERR will be asserted at the completion of the system reset.

INIT has no effect on a rewinding slave, but will immediately halt a slave that is executing any other command.

NOTE

Issuing an INIT during a write operation destroys the record being written. The only safe recovery from INIT is a rewind.

2.3.5 Read-In Preset

This command is intended to be used in bootstrap operations. Read-in preset does the following.

1. Presets the tape control register in the TM03 to select slave 0, odd parity, PDP-10 core dump format, and 800 bits/inch
2. Causes slave 0 to begin rewinding in accordance with the guidelines outlined in Paragraph 2.3.3

2.3.6 Erase

The selected slave writes an extended 7.6 cm (3 inch) interrecord gap and stops. ATA becomes asserted when DRY becomes asserted.

2.3.7 Write Tape Mark

The selected slave writes an extended 7.6 cm (3 inch) interrecord gap, an industry-compatible tape mark, and stops. ATA becomes aserted when DRY becomes asserted.

If a detectable tape mark was written (as is normally the case), TM (bit 2 of the status register) will be asserted at the completion of the operation.

2.3.8 Space Forward

The selected slave spaces forward (toward EOT) over the number of records specified by the contents of the frame count register. Detection of a tape mark (TM) or end of tape (END PT) causes a space command to be aborted. In this case, the frame count register reflects the number of records spaced over. (The register is not incremented by the tape mark.)

All data errors are inhibited during this operation. DRY becomes asserted when operation is complete and a valid interrecord gap found. ATA becomes asserted when DRY asserts.

Once the reflective marker indicating end of tape has been detected, it is possible to space forward *only* one record at a time. Attempts to space forward over more than one record (i.e., initiate space forward with a number other than -1 in the frame count register) will cause the transport to space over one record and halt, displaying frame count error in the error register.

2.3.9 Space Reverse

Space reverse is similar to space forward, except that detection of BOT or TM will abort the operation, and the direction of tape motion is in the reverse direction (toward BOT).

Whenever a space reverse is to be executed while END PT is asserted, it is advisable to space reverse over only one record at a time (as in Paragraph 2.3.8).

2.3.10 Read Forward/Write Check Forward

The tape system makes no distinction between these commands. The tape system reads one record. When either of these commands results in the detection of a tape mark, the following will occur.

1. In PE mode, no data transfers will be initiated by the TM03.
2. In NRZI mode, the TM03 will transfer both the tape mark character and its LRC character to the controller.

2.3.11 Read Reverse/Write Check Reverse

Read reverse/write check reverse is similar to read (write check) forward, with the following exceptions.

1. Data transfers occur as outlined in Paragraph 2.2.
2. Tape motion is in the reverse direction.
3. Regardless of mode, no data transfer will occur upon detection of a tape mark.

2.3.12 Write

In the write command, the transport writes one record while moving forward. The record length is controlled by the frame count register.

2.4 NRZI ERROR CORRECTION

Figure 2-9 is a simplified flow diagram of the error correction process. The process consists of three cycles.

1. Read the record in the forward direction and get a CRC error.

2. Read (or space) in reverse over the faulty record and attempt to compute the track in error.

3. If the track in error was computed (all errors are contained in a single track), make a forward read over the faulty record during which error correction is accomplished.

Figure 2-10 is a flow diagram of the NRZI error correction algorithm. During a NRZI read forward operation, data characters from tape are input into a CRC generator where a CRC character is developed. At the end of the record, the CRC character read from tape is compared to the generated CRC character. If a match is not obtained, a CRC error is asserted. The program then initiates the error correction process by changing the mode to reverse read or reverse space. The reverse space mode must be selected if it is desired to reverse the tape more than one record, e.g., to move the faulty record over the tape cleaner. If a reverse read was in progress when the CRC error was detected, the mode must be changed to forward read and the faulty record read again. The error correction process can be initiated only when a CRC error is sensed in a forward direction.

As the faulty record is reverse read (or reverse spaced), the track in error is computed. If more than one track is in error, the hardware will not select a faulty track and the error is determined to be uncorrectable. If the errors are all in the same track, a track in error is computed. In either case, the correction cycle portion of the error correction process is performed.

When the correction cycle is started, the tape must be positioned at the correct location (i.e., at the faulty record) so that the error correction is performed on the proper record. If the read reverse mode was chosen in the preceding paragraph, only one record (the faulty record) can be reverse read. An attempt to read reverse more than one record causes the hardware to abort the error correction process. If the space reverse mode was chosen, any number of records may be spaced while the error correction process is put on "hold." If the program spaced N records in reverse, it must space N–1 records forward before read forward is asserted. (The assertion of read forward initiates the correction cycle portion of the process.) Otherwise, the hardware will attempt the error correction on the wrong record.

If the error is uncorrectable, no correction will be accomplished during the correction cycle. The faulty record is reread and CRC error is again asserted. In this case, software retry procedures or other corrective action the program may direct will be instituted.

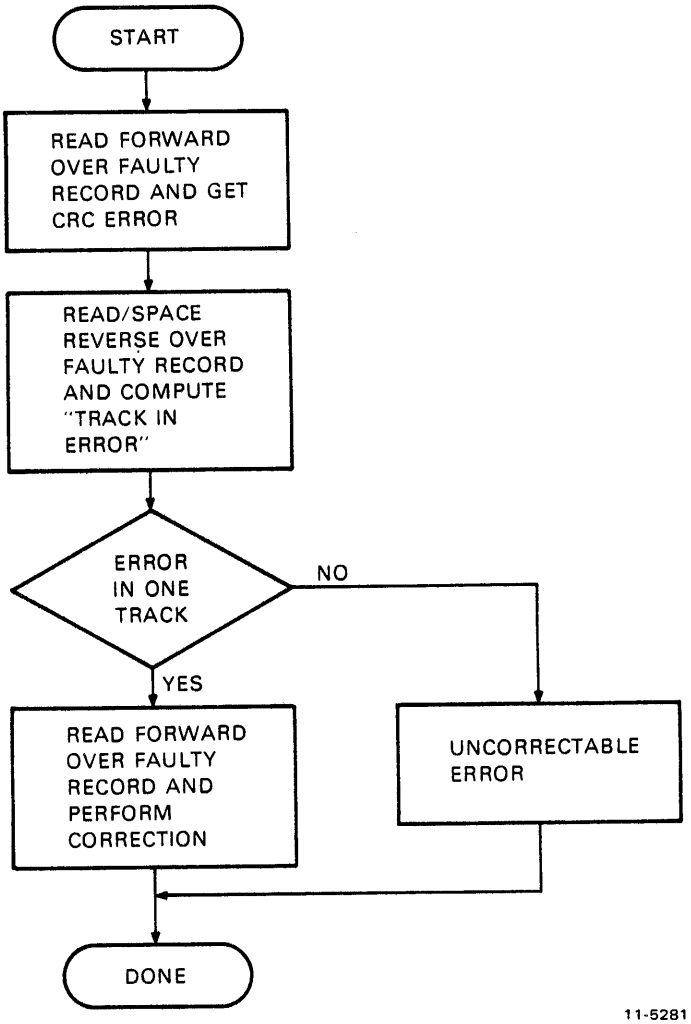


Figure 2-9 Simplified NRZI Error Correction Flow Diagram

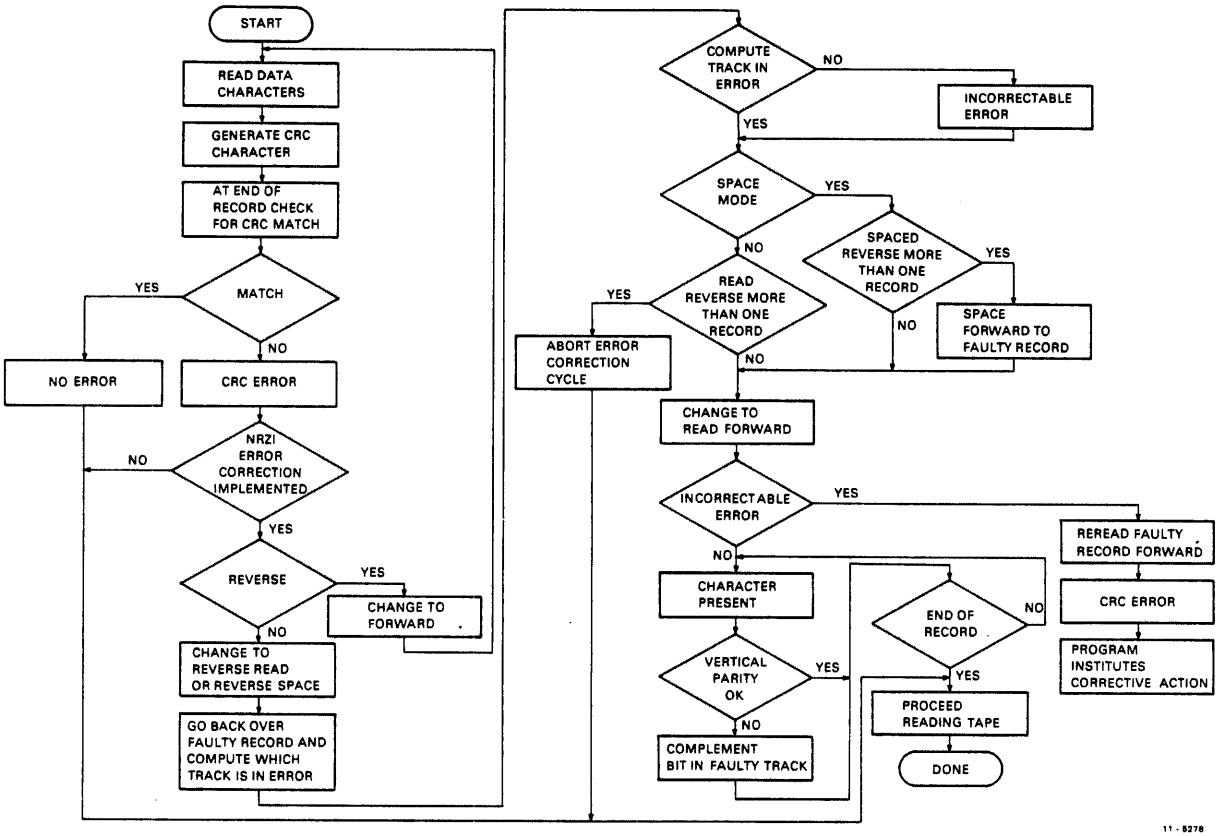


Figure 2-10 NRZI Error Correction Flow Diagram

If an erroneous track was detected, correction is accomplished during the correction cycle. This is done by checking each character for vertical parity. Any character having a vertical parity error has the bit corresponding to the track in error complemented. Thus, any number of errors are corrected so long as they all occur in the same track.

When the end of record is sensed, the error correction process is terminated and the reading operation is continued. It is significant to note that the CRC character is treated as part of the record and, therefore, is checked for vertical parity and, if necessary, corrected.

2.5 PROGRAMMING NOTES

Points to consider in programming the TM03 formatter are listed below.

2.5.1 NRZI Error Correction

1. If in reverse read when a CRC error is sensed, the mode must be changed to forward read. The error correction process is entered only when a CRC error is sensed in a forward direction.
2. When a forward CRC error is sensed, the direction must be changed to reverse to initiate the error correction process.
3. If reverse read is used in item 2 above, only one record can be read and then the direction must be changed to forward read.
4. If reverse space is used in item 2 above, any number of records (N) may be reverse spaced; however, N-1 records must be forward spaced before forward read is asserted.
5. If the error is uncorrectable, the program must dictate any corrective action.

2.5.2 Auto Density Select

1. The program does not control the read mode (density). The presence or absence of an ID burst on the tape selects either PE read or NRZI read for the entire tape.
2. The program can select either write PE or write NRZI at BOT but cannot switch modes at a later point on the tape.
3. If the mode (density) is changed and a rewind off-line command is given, a nonexecutable function error will result.

2.5.3 Other Notes

1. All slaves interfacing to a particular TM03 must be operating at the same speed.

CHAPTER 3
INSTALLATION

3.1 SITE PLANNING AND CONSIDERATIONS

Since the TM03 is always contained within a transport cabinet, the site planning aspects are accomplished when site planning for the cabinet is considered. The additional power required to supply the TM03 is 300 W.

3.2 UNPACKING

There are no unpacking instructions for the TM03 since it is shipped already mounted inside the transport cabinet. The TM03 cables may be shipped separately and are the only items that must be unpacked.

3.3 INSPECTION

Check inside the transport cabinet that the TM03 is securely mounted on its platform and that there is no apparent damage to the TM03 housing. Check that there are the proper number of BC06R-X cables of the correct length for the particular installation (X = length of cable). Check cables for damage both at the connectors and over the length of the cable body.

3.4 INSTALLATION PROCEDURES

Installation consists of cabling up either six or nine BC06R cables to the TM03. The number of cables depends on the number of TM03s in the system and the type of cabinet used. Three cables couple in the Massbus from the controller. Three more cables carry the Massbus out to the next TM03. If there is only one TM03 in the system, the Massbus may be terminated in the TM03 in which case the three "out" cables are not used. The last three cables carry the slave bus to the first slave transport, which is actually housing the TM03.

If the TM03 cables are already installed, there is no TM03 installation required; therefore, use the following instructions as applicable.

3.4.1 TM03 Cabling

1. Slide the TM03 out of the cabinet as shown in Figure 3-1.
2. Unscrew the two cover fasteners and remove the module cover.
3. Remove the six connector modules: M8937, M8908-YA, M8908, and the three M59903s.*
4. Connect the three BC06R Massbus cables (MBA, MBB, and MBC) to the IN jacks on the three M5903* cards as shown in Figures 3-2, 3-3, and 3-4. Orient the connectors so that the smooth side of the cable is up and the colored stripes on the cables are toward the module handles (Figure 3-1).

*May be M5903-YAs.

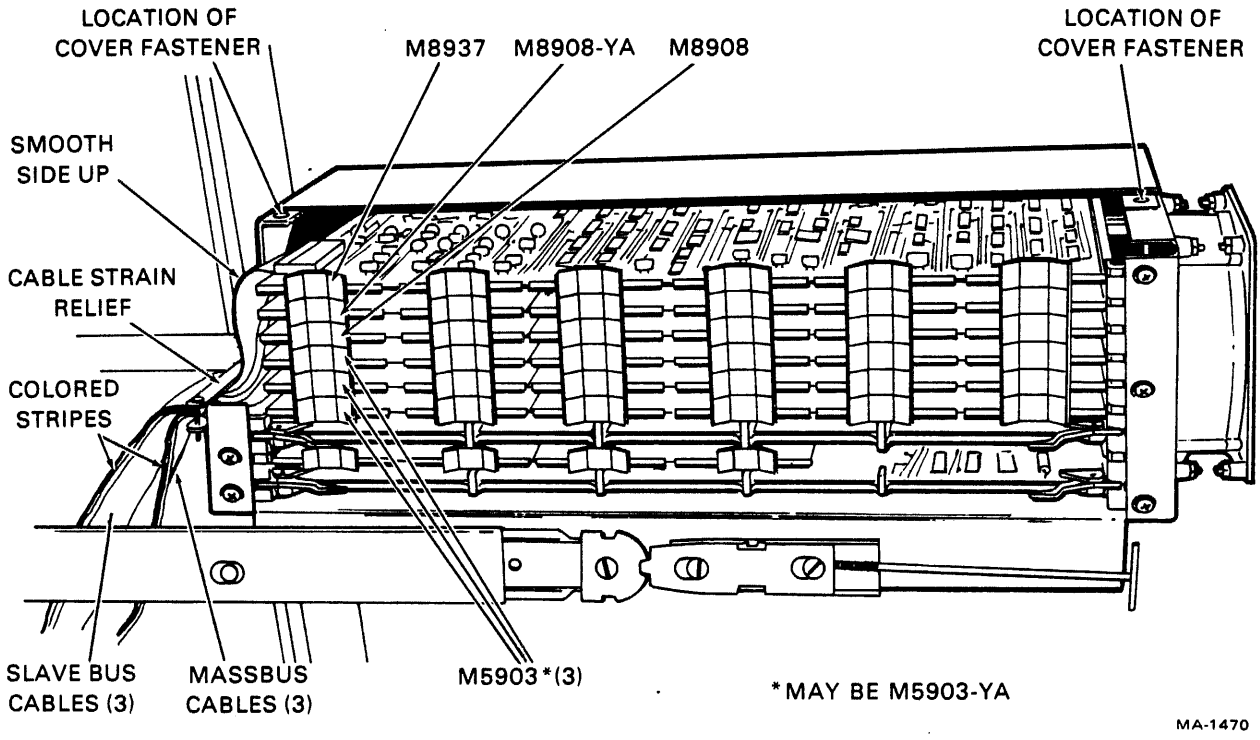
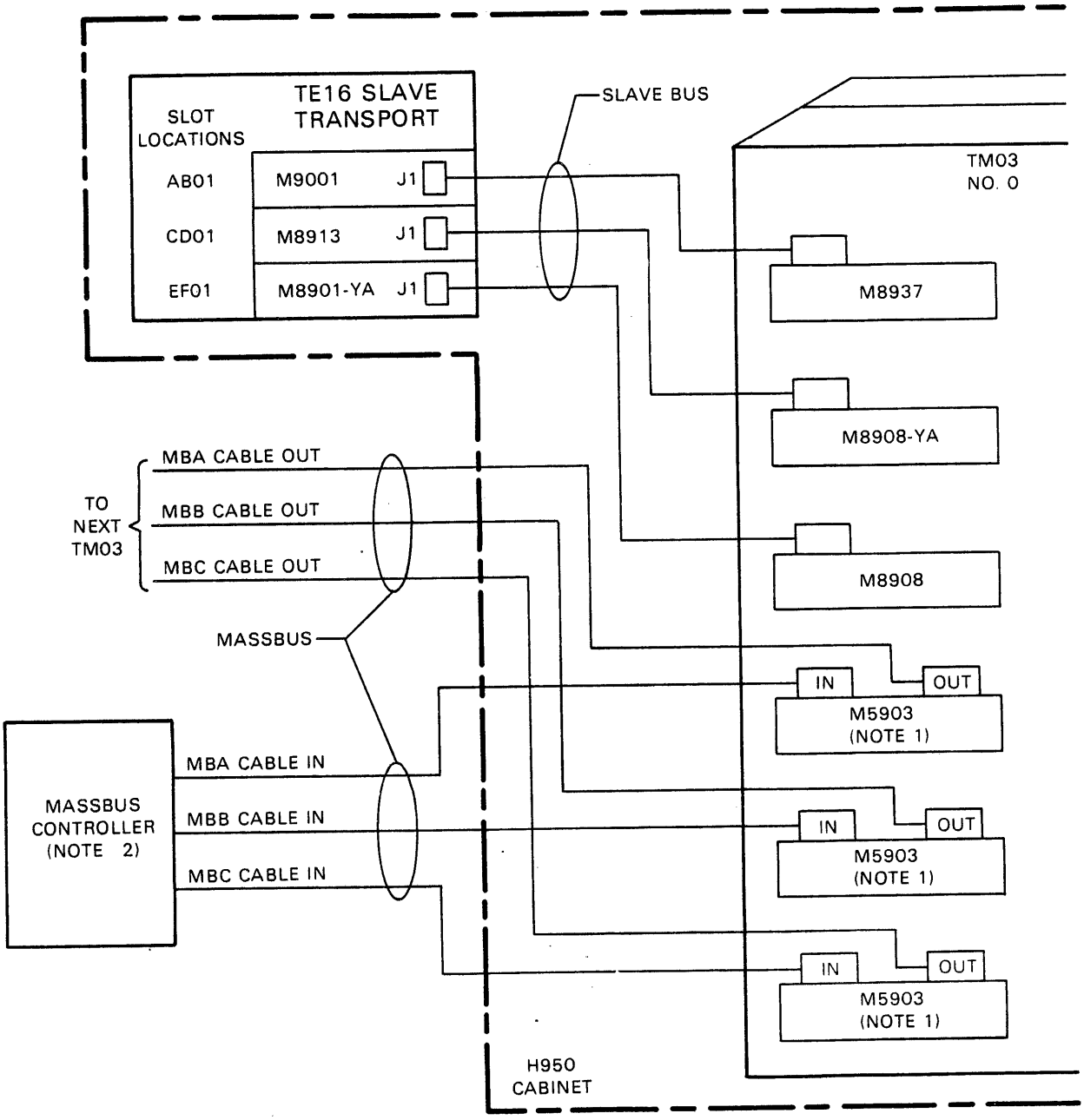


Figure 3-1 TM03 Formatter with Cover Removed



NOTES:

1. IF ONLY ONE TM03 IS USED IN SYSTEM, AN H870 TERMINATOR IS INSERTED INTO EACH OUT JACK, OR M5903-YA MODULES ARE USED WHICH PROVIDE MASSBUS TERMINATION.

2. RH10, RH11, RH20, RH70 OR RH780

MA4087

Figure 3-2 TM03 Cabling to a TE16 Slave Transport in an H950 Cabinet

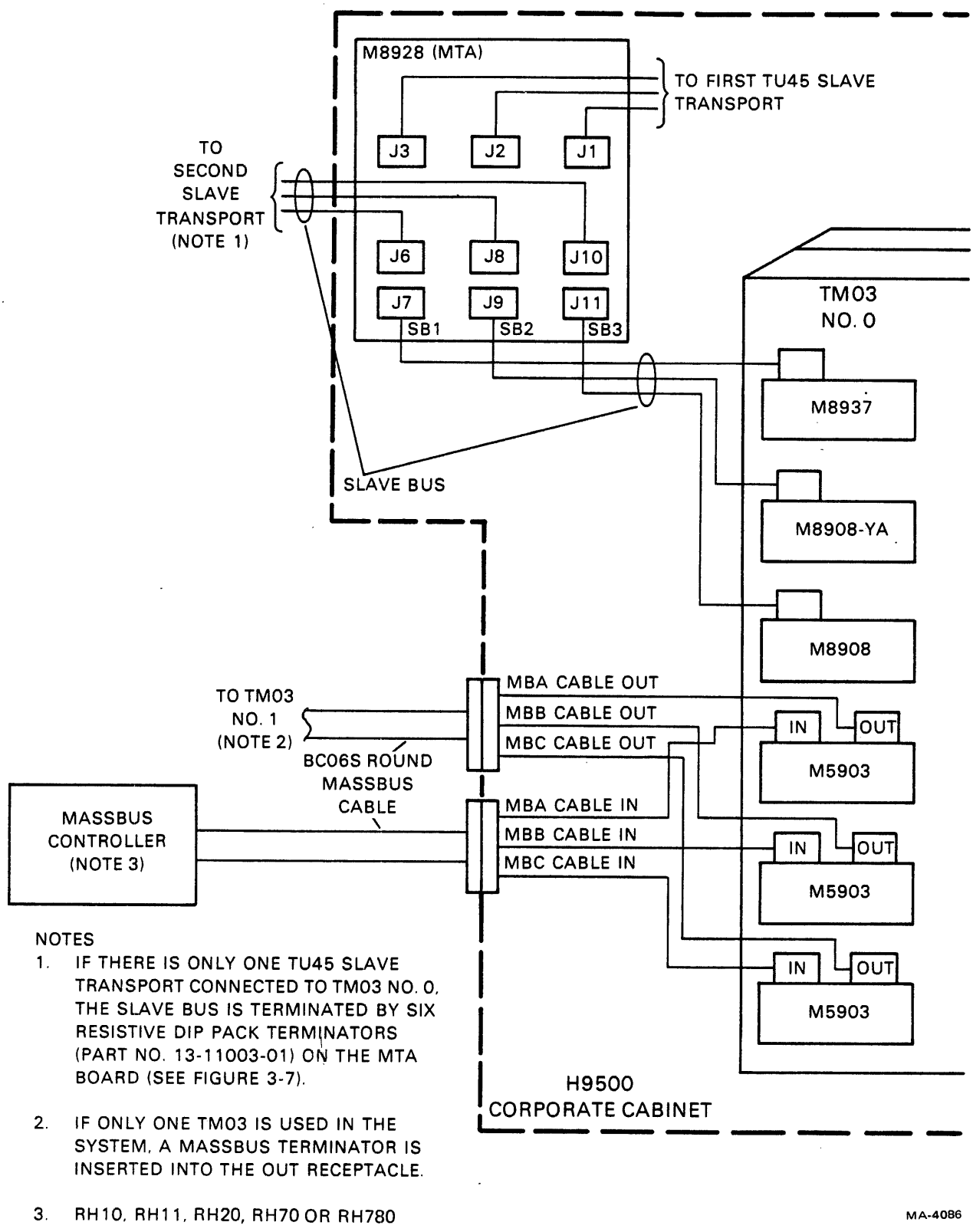


Figure 3-3 TM03 Cabling to an M8928 MTA Adapter Board in a TU45 Transport in an H9500 Corporate Cabinet

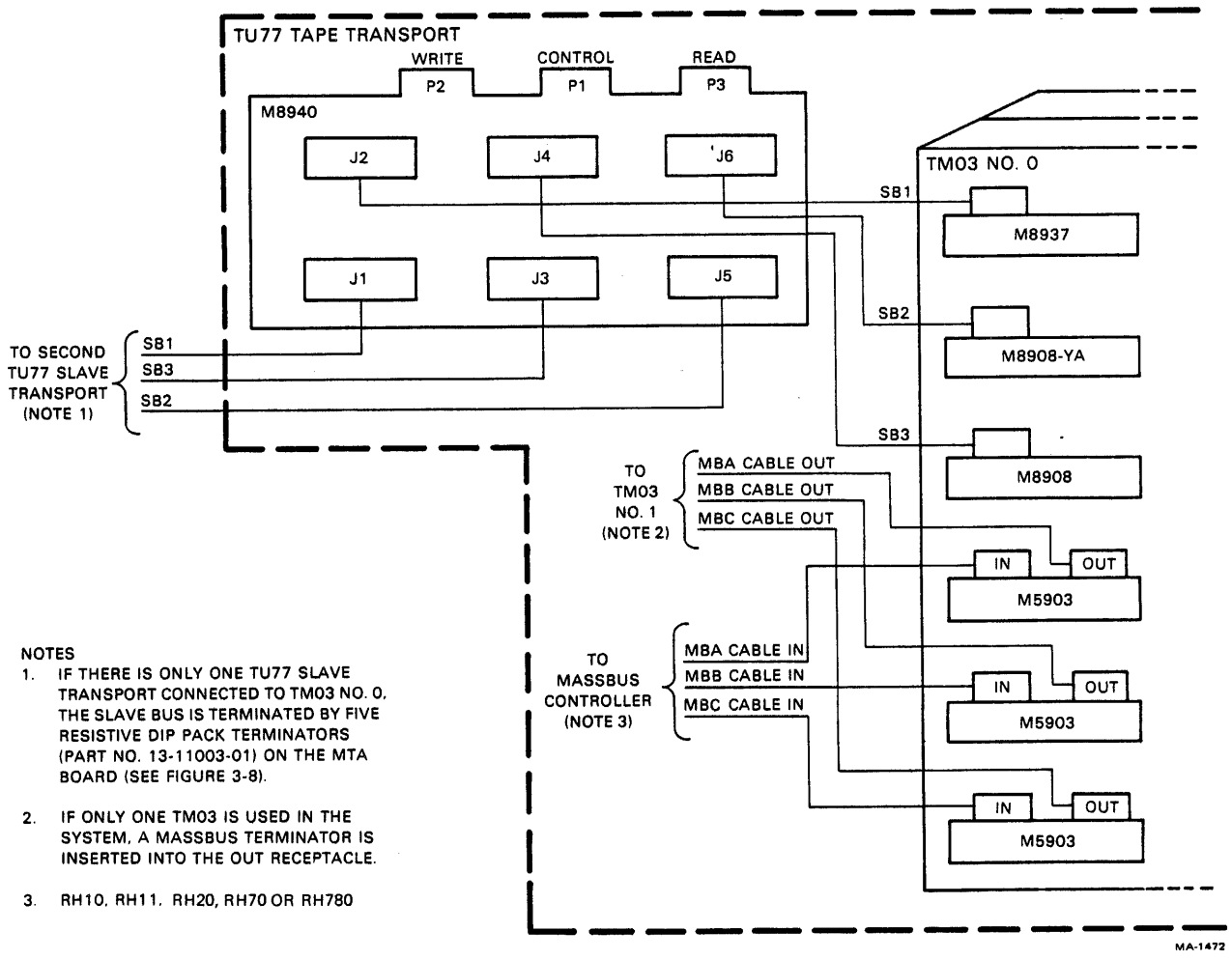


Figure 3-4 TM03 Cabling to an M8940 MTA Adapter Board in a TU77 Transport in an H9500 Corporate Cabinet

5. If another TM03 is to be daisy-chained onto this one or if the TM03 is housed in a H9500 corporate cabinet, connect three BC06R cables to the OUT jacks on the three M5903* boards. The orientation of the three "out" cables is ribbed side up but with the colored stripe still toward the module handles.

6. If only one TM03 is used in the system and it is housed in a 48.3 cm (19 inch) H950 cabinet, insert an H870 terminator into each OUT jack or ensure that the Massbus cable cards are M5903-YAs.

7. Insert the three M5903* cards into the TM03, working from the bottom up, i.e., MBC cable card first.

8. Connect three BC06R slave bus cables to the jacks on modules M8908, M8908-YA, and M8937. Orient the connectors as in step 4, i.e., smooth side of cable up and colored stripes toward the module handles.

9. Insert the three connector modules into the TM03 working from the bottom up, i.e., M8908 first and M8937 last.

10. Secure the cable strain relief over the six BC06R cables as shown in Figure 3-1.

3.4.2 Massbus Cabling to Transport Cabinet

NOTE

In cabling up the Massbus, note that the maximum allowable length of the Massbus when used with TM03s is 36.9 m (120 ft).

3.4.2.1 H950 Cabinet - Massbus cabling to the 48.3 cm (19 inch) H950 cabinet is usually via flat BC06R ribbon cables. The cables connect directly from the controller to the TM03 where the Massbus is either terminated or daisy-chained to the next TM03. Figure 3-2 illustrates this type of hookup.

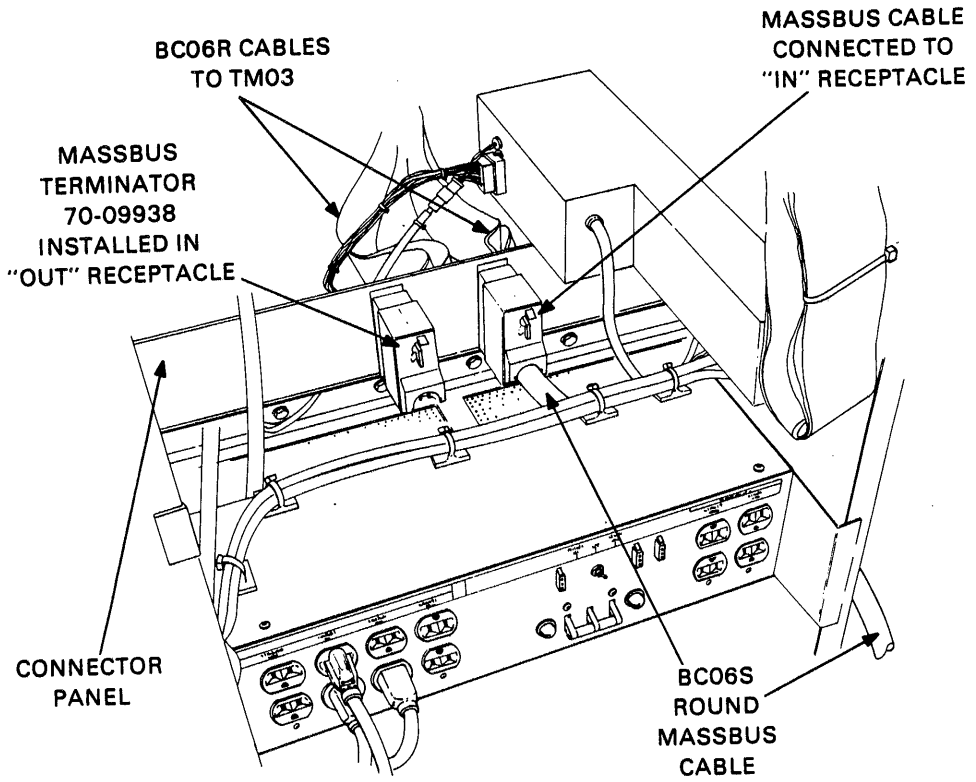
3.4.2.2 H9500 Corporate Cabinet - Massbus cabling to the short H9500 corporate cabinet is via round BC06S cable which connects to a panel in the lower section of the TU45 cabinet (Figures 1-3 and 3-5a) and to the rear of the TU77 cabinet (Figure 3-5b). Three BC06R flat cables connect the Massbus from the "in" receptacle on the connector panel to the TM03. Three more cables carry the Massbus from the TM03 to the "out" receptacle on the connector panel where it is either terminated by a Massbus terminator (P/N 70-09938) or daisy-chained to the next H9500 cabinet via the BC06S round cable. Figures 3-3 and 3-4 illustrate this type of hookup.

The BC06R cabling to the connector panel is shown in Figure 3-6. Note that cables MBA through MBC are installed from right to left on both the "in" and the "out" receptacles. Observe the smooth side/ribbed side and colored-stripe orientation shown in the figure.

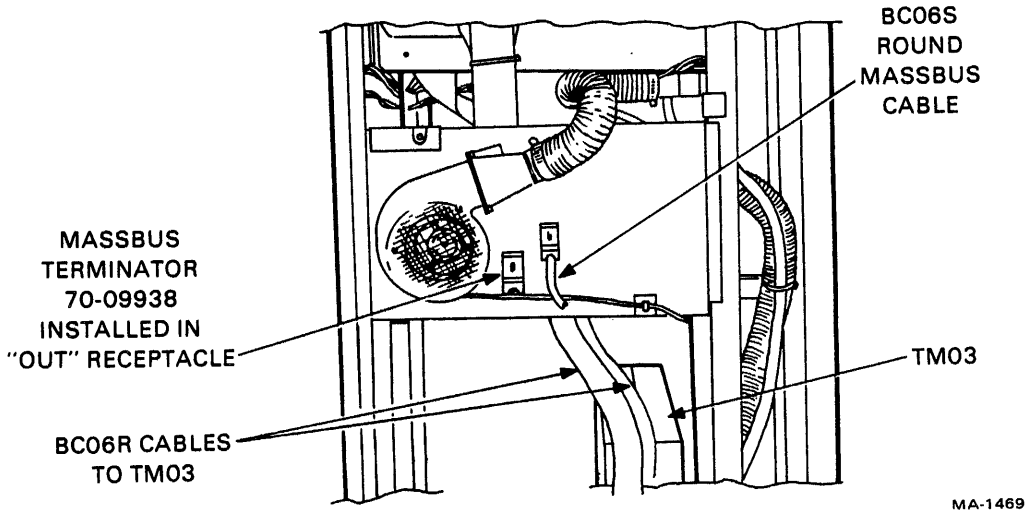
3.4.3 Slave Bus Cabling to Tape Transport

3.4.3.1 TE16 Transport - For cabling to a TE16 slave transport, connect the three slave bus cables to J1 on the TE16 cable cards (M9001, M8913, M8901-YA) as shown in Figure 3-2. Refer to the TE16/TE10W/TE10N user or maintenance manual (Paragraph 1.4) for cabling instructions and orientation on the TE16 cable cards.

*May be M5903-YAs.



a. Connector Panel in TU45 Transport



b. Connector Panel in TU77 Transport

Figure 3-5 External Cabling to Massbus Connector Panel in H9500 Corporate Cabinet

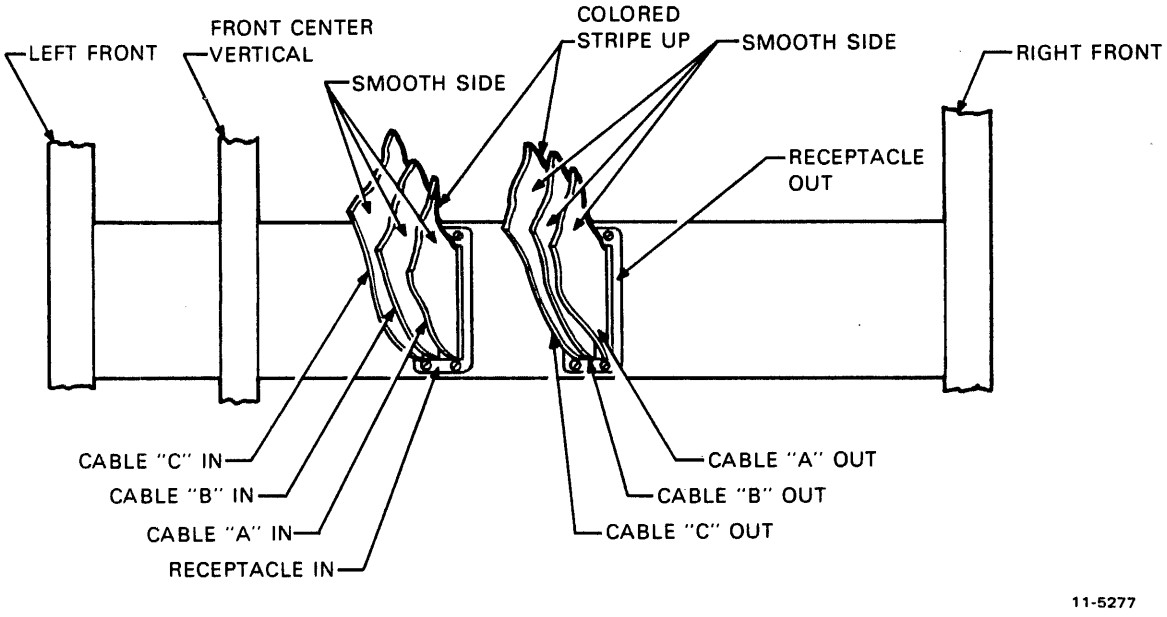


Figure 3-6 Internal Cabling to
Massbus Connector Panel in H9500 Corporate Cabinet

3.4.3.2 TU45 Transport - An M8928 magnetic tape adapter board (MTA) is used to interface the TM03 to a TU45 tape transport. The MTA board is located on a shelf just above the TM03 (Figure 1-3). To cable up the M8928 MTA board, connect the three BC06R slave bus cables from the TM03 to J7, J9, and J11 as shown in Figures 3-3 and 3-7. Insert the connectors so that the cable's smooth side is up and the colored stripe is on the left as shown in Figure 3-7. The three cables connecting to the first slave transport (which houses the TM03) are type BC08R and connect to J1, J2, and J3. The BC08R cables are also connected with the smooth side up and the colored stripe on the left.

If there is only one slave transport connected to TM03 No. 0, terminate the slave bus by inserting six resistive DIP packs (P/N 13-11003-01) into the MTA board. If another slave transport is daisy-chained onto TM03 No. 0, connect three BC06R slave bus cables to J6, J8, and J10. These three cables are connected with the ribbed side up but with the colored stripe still on the left (Figure 3-7).

Refer to the TU45A maintenance manual for additional cabling information (Paragraph 1.4).

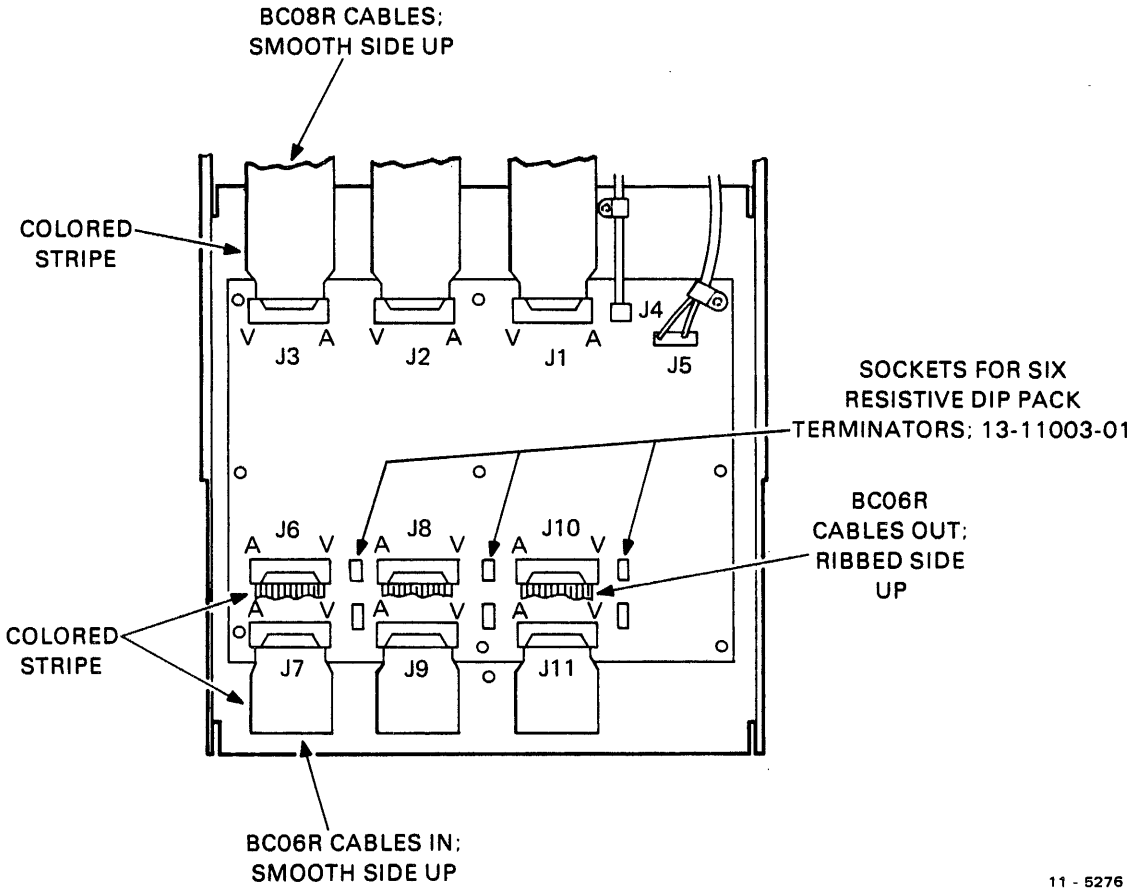


Figure 3-7 Cable Orientation on M8928 MTA Module

3.4.3.3 TU77 Transport – An M8940 magnetic tape adapter board (MTA) is used to interface the TM03 to a TU77 tape transport. The MTA board is plugged into the card cage assembly inside the TU77 cabinet. To cable up the M8940 MTA board, connect the three BC06R slave bus cables from the TM03 to J2, J4, and J6 as shown in Figures 3-4 and 3-8. Insert the connectors so that the cable's smooth side is facing to the rear and the colored stripe is on the left as shown in Figure 3-8.

If there is only one slave transport connected to TM03 No. 0, terminate the slave bus by inserting five resistive DIP packs (P/N 13-11003-01) into the MTA board as shown in Figure 3-8. If another slave transport is daisy-chained onto TM03 No. 0, connect three BC06R slave bus cables to J1, J3, and J5. These three cables are connected with the ribbed side facing to the rear but with the colored stripe still on the left (Figure 3-8).

Refer to the TU77 user's guide or technical manual for additional cabling information (Paragraph 1.4).

3.5 ACCEPTANCE TESTING

The acceptance tests for the TM03 are the same as those for the particular transport being used with the TM03. If the transport acceptance tests are performed satisfactorily, then the TM03 has been installed and is operating properly. See Paragraph 1.4 for documents pertaining to the various transports that can interface with the TM03. Acceptance tests for the various transports are found in these documents.

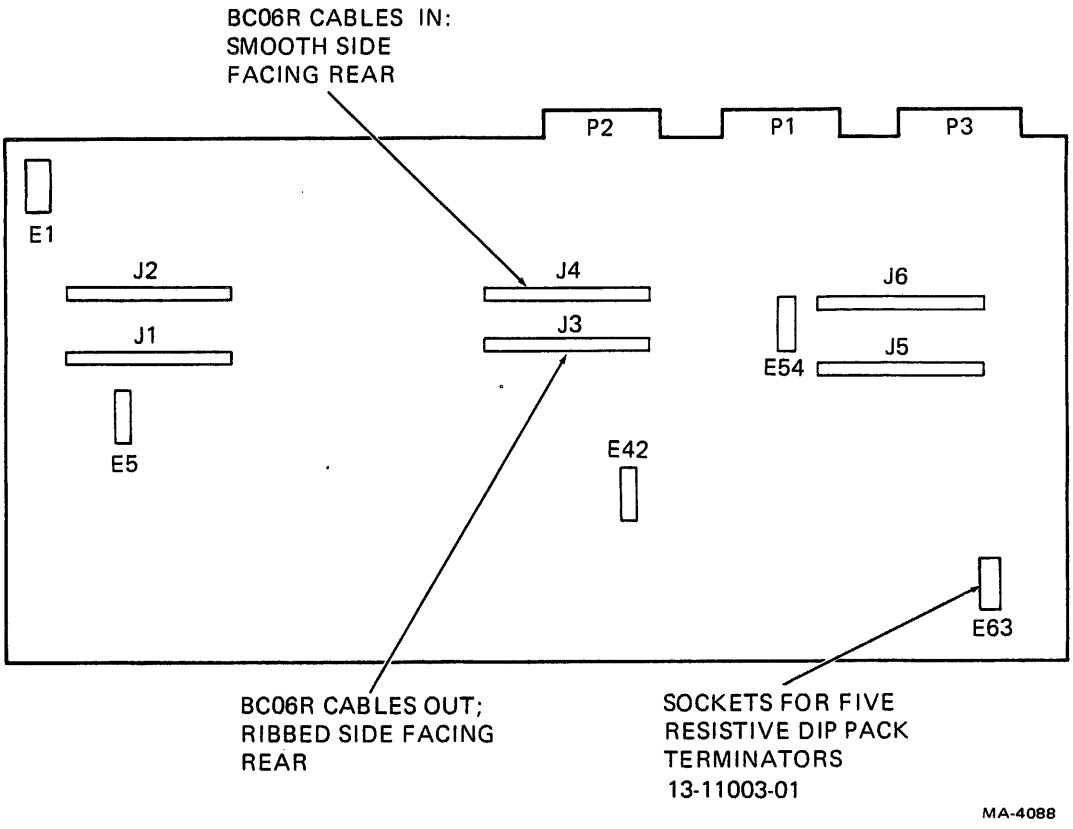


Figure 3-8 Cable Orientation on M8940 MTA Module

CHAPTER 4
THEORY OF OPERATION

4.1 GENERAL OPERATION

The functional description contained in Chapter 1 gives a brief overview of the TM03 tape formatter. The discussions contained in Paragraph 4.1 are still of a general nature but are more detailed than that contained in Chapter 1. The write data path and read data path are discussed separately as distinct operations. In addition, each of the eight commands that the TM03 can process is discussed separately as an operational sequence with a corresponding flowchart. Some redundancy exists among the descriptions of the operational sequences in order to keep each of the eight sequences separate.

Figure 4-1 and Tables 4-1 and 4-2 illustrate and define all the signals on the Massbus and the slave bus. Refer to them throughout the discussions of Chapter 4.

4.1.1 Write Data Path

The write data path, shown in the TM03 block diagram (Figure 1-7), is discussed in this section in greater detail (Figure 4-2).

To write data on tape, the Massbus controller, after loading the tape control register and the frame count register, loads the write data function code into the control register, places data on the data bus, and asserts RUN H to the TM03. When the TM03 is ready to accept a data word, it asserts SCLK to the Massbus controller, which responds by asserting WCLK to the TM03.

Table 4-1 Massbus Interface Signals

Signal	Function
Data Bus	
Data Lines [D(0:17)]	These bidirectional lines transmit 18 parallel data bits to or from the TM03.
Data Lines Parity (DPA)	This bidirectional line transmits the data parity bit (odd parity) to or from the TM03. Data parity is simultaneously transmitted with the bits on the data lines.
Sync Clock (SCLK)	During a data write, this line transmits SCLK from the TM03 to request write data from the Massbus controller. During a data read, this line transmits SCLK to the Massbus controller to indicate that read data is present on the data lines.
Write Clock (WCLK)	During a data write, this line transmits WCLK from the Massbus controller to strobe write data into the TM03.

Table 4-1 TM03 Interface Signals (Cont)

Signal	Function
Run (RUN)	This line transmits RUN from the Massbus controller to initiate data transfer execution.
End of Block (EBL)	Normally, this line transmits EBL from the TM03 at the end of each record. However, for certain abnormal conditions where it is necessary to terminate the transport operation immediately, EBL is transmitted prior to the end of the record.
Exception (EXC)	This bidirectional line transmits EXC from the TM03 to indicate that an error has occurred during data transfer. In some systems, EXC H can also be transmitted over this line from the controller to abort an in-progress data transfer.
Occupied (OCC)	During a data transfer (read/write), this bidirectional line transmits OCC from the TM03 to indicate that a transport has control of the data bus. Once asserted, this signal prevents any other transport from using the data bus.
Control Bus	
Control Lines [C(0:15)]	These bidirectional lines transmit 16 parallel control or status bits to or from the TM03.
Control Lines Parity (CPA)	This bidirectional line transmits control lines parity (odd parity) to or from the TM03. Control parity is simultaneously transmitted with the bits on the control lines.
Drive Select [DS(0:2)]	These three lines transmit a 3-bit binary code from the Massbus controller to select a particular TM03.
Register Select [RS(0:4)]	These five lines transmit a 5-bit binary code from the Massbus controller to select one of the ten TM03 registers.
Controller to Drive (CTOD)	This line transmits the CTOD signal from the Massbus controller to indicate in which direction data is to be transferred on the control lines. For a controller-to-drive transfer, the controller asserts CTOD. Conversely, for a drive-to-controller transfer, the controller negates CTOD.
Demand (DEM)	This line transmits DEM from the Massbus controller to initiate a control bus transfer (initiate "handshake").
Transfer (TRA)	This line transmits TRA from the TM03 in response to DEM. The assertion of TRA indicates that data is available on the control bus.
Attention (ATTN)	This line transmits ATTN from the TM03 to indicate that a nontransfer error or transport status change has occurred.

Table 4-1 TM03 Interface Signals (Cont)

Signal	Function
Initialize (INIT)	This line transmits INIT from the Massbus controller to initialize all TM03s and transports on the daisy chain. INIT is transmitted at system startup or whenever the Massbus controller issues an initialize command.
Massbus Fail (MASSFAIL)	This line transmits MASSFAIL L negated from the Massbus controller to indicate that the controller power supply is operating properly. If the controller power supply fails, MASSFAIL L is asserted, thus initializing the TM03 logic as well as preventing it from accepting erroneous control bus information.

Table 4-2 Slave Bus Interface Signals

Signal	Function
Slave Select [SS(0:2)]	These lines select one of eight possible transports for command execution.
Forward (FWD) Reverse (REV) Rewind (RWND) Write Enable (WRITE)	These are the four command lines which determine transport operation.
Slave Set Pulse (SLAVE SET PLS)	This signal initiates transport response to the four command lines.
Stop (STOP)	This signal causes the transport to terminate motion. (Does not apply to rewind, which terminates independently.)
Enable Motion Delay (EMD)	This signal enables the transport to gate out a coded motion delay preset onto the read lines.
Accelerate (ACCL)	This signal is asserted by the TM03 while the transport is getting up to speed or not moving tape. It is not asserted while the IDB is being written.
Write Data [WD(0:7,P)]	These nine lines transmit data to be written by the slave transport.
Record (REC)	This pulse causes data to be written on tape.
Density Select (DEN0, DEN1, DEN2)	These three lines control the density at which data is written onto or read from tape. DEN 2 is the only line presently being used.

Table 4-2 Slave Bus Interface Signals (Cont)

Signal	Function
Clock (CLOCK)	This clock, generated in the transport, is present at all times when the transport is selected, loaded with tape, and on-line. The frequency of CLOCK depends on the transport tape speed [144 kHz for 114.3 cm/second (45 in/second) slaves; 240 kHz for 190.5 cm/second (75 in/second) slaves; 400 kHz for 317.5 cm/second (125 in/second) slaves].
Write Clock (WRT CLK)	This clock is transmitted to the TM03 by a powered, selected, on-line transport loaded with tape when it is running at speed (ACCL not asserted). The frequency of WRT CLK is a function of the DEN lines and of the transport tape speed, and controls the write timing frequency.
LRC Strobe (LRC STRB)	Asserted by the TM03 prior to the REC pulse that writes the LRC character.
Read Data [RD(0:7,P)]	These nine lines transmit read data from the transport to the TM03. (They also transmit the motion delay preset.)
Read Strobe Delay Over (RSDO)	A read strobe pulse generated by the transport at the end of the skew delay in NRZI mode.
Set Vertical Parity Error (SET VPE)	Not Used. Tied to +dc.
Beginning of Tape (BOT)	Asserted when the transport detects the beginning-of-tape marker.
End of Tape (END PT)	Asserted when the transport detects the end-of-tape marker.
Rewind Status (RWS)	Asserted while the selected transport is performing a rewind operation.
7-Channel (7 CH)	Always negated by a selected transport.
Slave Present (SPR)	Asserted by a selected, powered transport.
Medium On-Line (MOL)	Asserted by a selected, powered transport which is loaded with tape.
Tape Unit Ready (TUR)	Asserted by a selected transport to indicate that tape motion has stopped.

Table 4-2 Slave Bus Interface Signals (Cont)

Signal	Function
Settle Down (SDWN)	Asserted while the transport is decelerating, until it has stopped.
Phase Encoded Status (PES)	Asserted by a transport when instructed to operate in PE mode.
Slave Attention (SLA)	Asserted by a transport when it comes on-line.
Set Slave Status Change (SET SSC)	Asserted at the completion of a rewind and when the transport comes on-line. It is also pulsed when the transport goes off-line or when the transport power fails. This line may be asserted by any slave, selected or not. Cleared by INIT or DRV CLR PLS.
Write Lock (WRL)	Asserted when the selected transport detects that the write enable ring has been removed from the tape reel.
Interchange Read (IRD)	A maintenance function. When asserted in NRZI mode, skew delays are tightened; in PE mode, on-the-fly error correction is inhibited.
Drive Type [DT(0:2)]	Specifies the type of slave transport as follows: DT2 | DT1 | DT0 | Type 0 | 0 | 0 | Unselected slave 0 | 0 | 1 | 114.3 cm/s (45 in/s) slave 0 | 1 | 0 | 190.5 cm/s (75 in/s) slave 1 | 0 | 0 | 317.5 cm fs (125 in/s) slave
Serial Number [SN(0:15)]	These 16 lines contain the BCD code of the last four digits of the serial number of the selected transport.
Drive Clear Pulse (DRV CLR PLS)	When asserted by the TM03, DRV CLR PLS clears SLA and SET SSC in the selected slave.
Initialize Pulse (INIT PLS)	When asserted by the controller, INIT PLS L clears SLA and SET SSC, and terminates tape motion (except rewinds) in all on-line transports.
+5 V	The TM03 supplies this voltage to power the slave bus terminator networks.

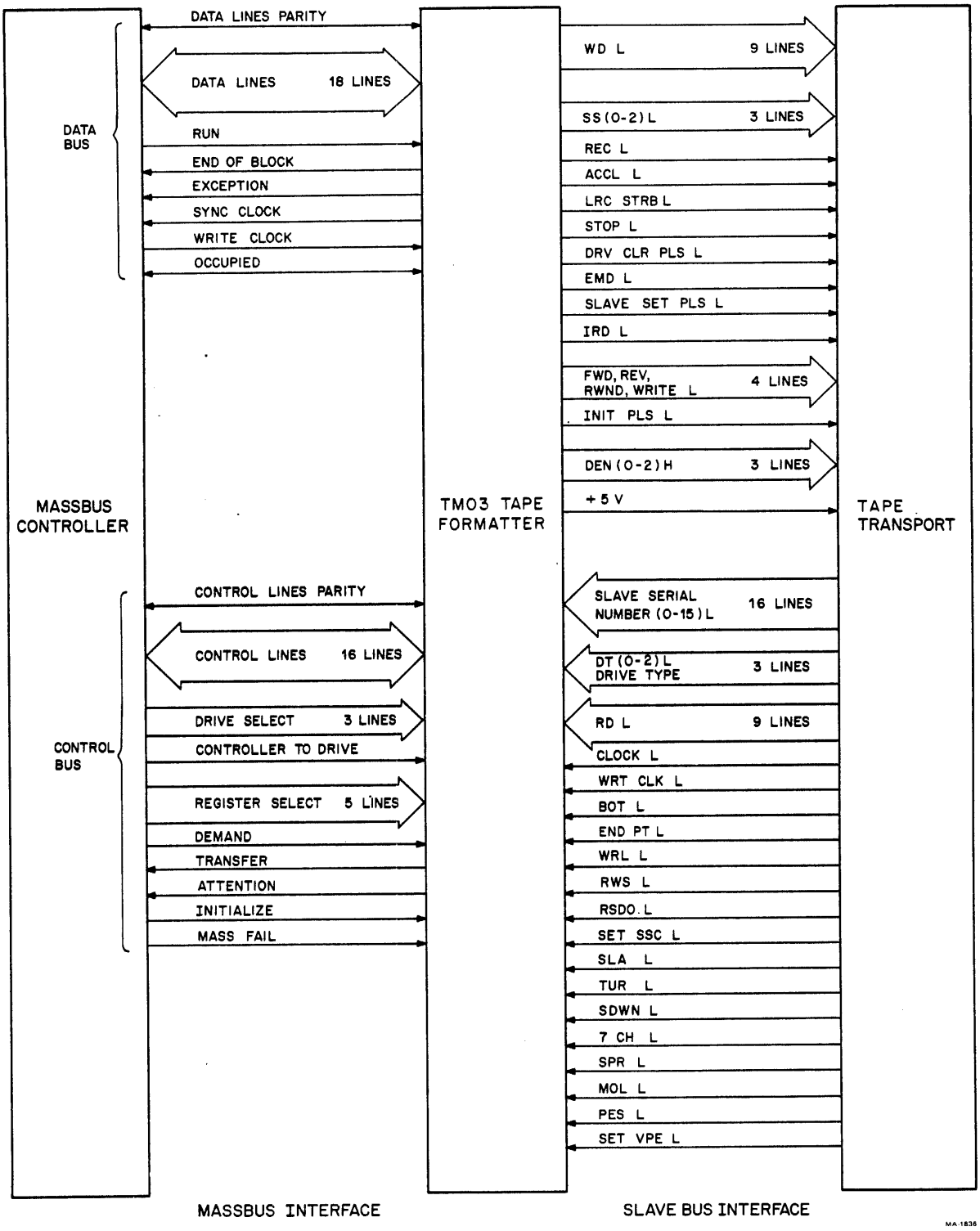


Figure 4-1 TM03 Interface Signals

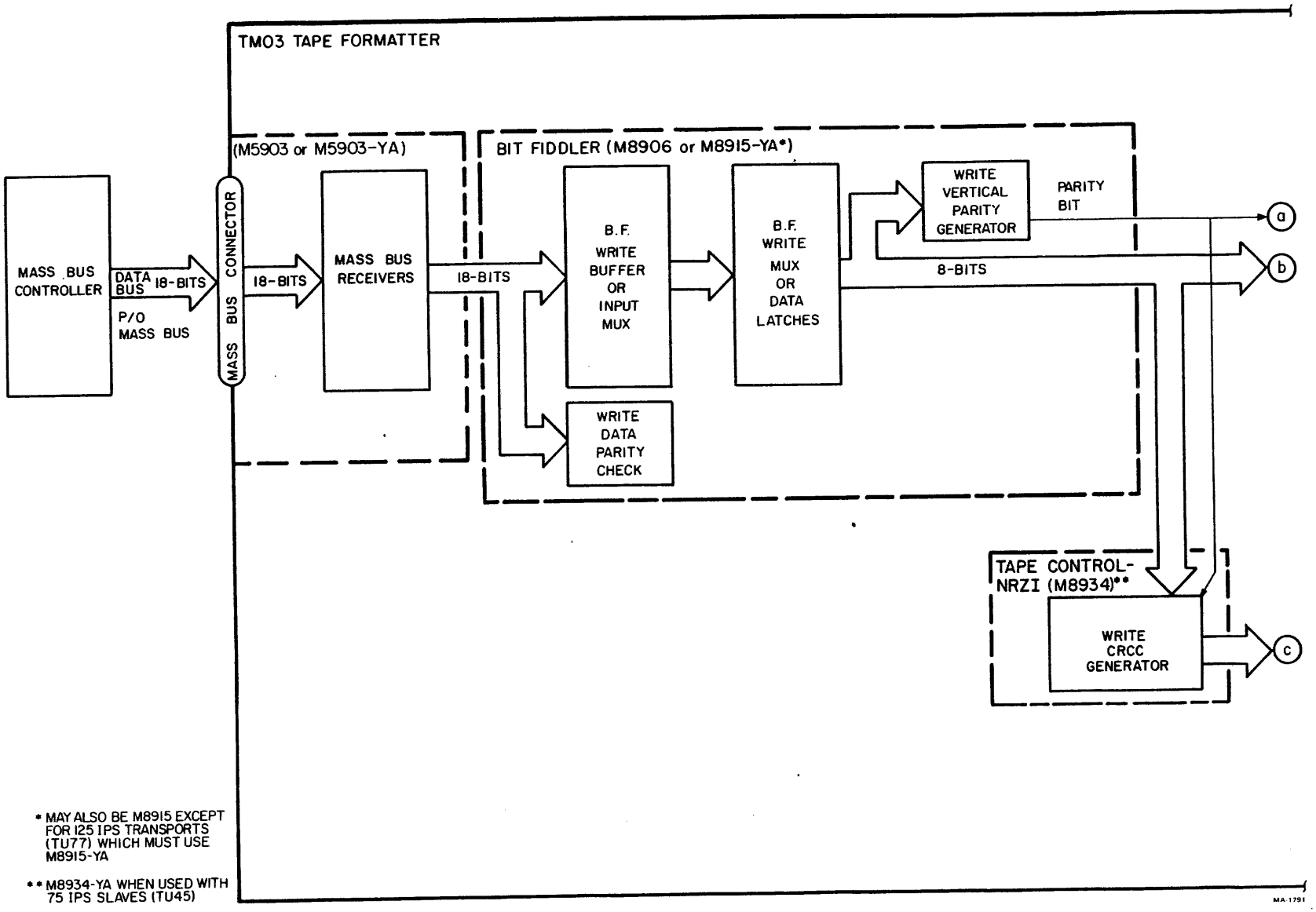


Figure 4-2 Write Data Path (Sheet 1 of 2)

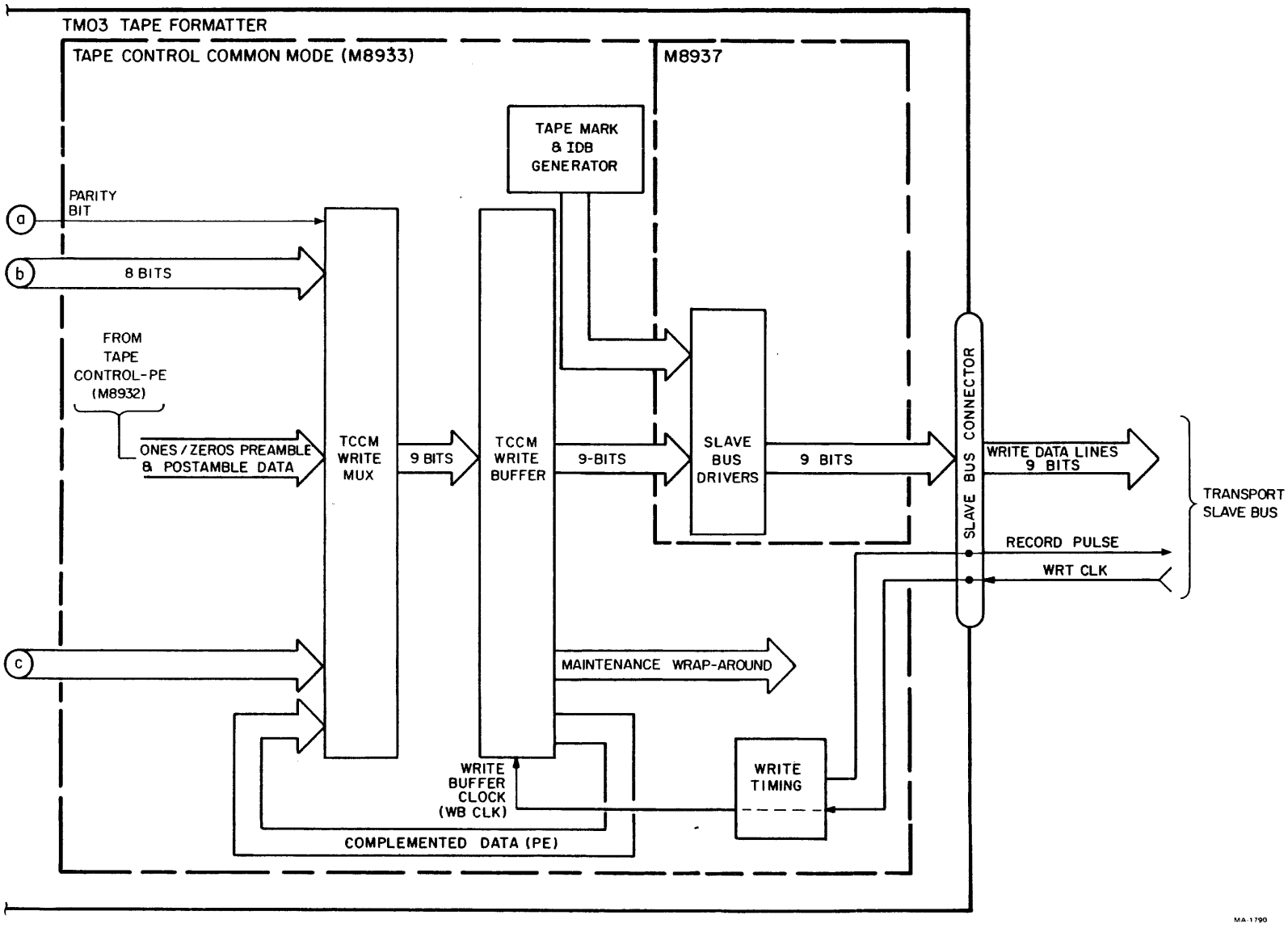


Figure 4-2 Write Data Path (Sheet 2 of 2)

The data word, transmitted over the Massbus, is received in the TM03 by the Massbus receivers (M5903) and applied to the bit fiddler write buffer (or input multiplexer on M8915-YA). When WCLK is received by the TM03, the data word is strobed into the buffer (or input multiplexer). A parity check is also performed on the input data. The bit fiddler write multiplexer (or data latches) then disassembles the data word by multiplexing different portions of the word onto the eight write data bit fiddler output (WDBFO) lines, and generates a vertical parity bit for each 8-bit character output. Some of these lines may not contain true data, but may be forced high or low to conform to the format in which data is to be written on tape. The manner in which the bit fiddler operates will be determined by the format bits in the tape control register.

The outputs of the bit fiddler are input to the tape control common mode (TCCM) module (M8933). The bit fiddler outputs, including the vertical parity bit, are one set of inputs to the TCCM write multiplexer.

The bit fiddler outputs, including the vertical parity bit, are also input to the write CRCC generator on the tape control-NRZI module (M8934 or M8934-YA) where in NRZI mode, they generate the CRCC that will be written on the tape at the end of the record. The outputs of the CRCC generator are another set of inputs to the TCCM write multiplexer.

A third set of inputs to the TCCM write multiplexer comprises the all 1s/0s preamble and postamble data. These inputs are controlled by the tape control-PE circuitry (M8932), and are selected by the TCCM write multiplexer when the PE preamble or postamble is written. They cause the all-1s and all-0s characters of the PE preamble and postamble to be written.

The fourth set of inputs to the TCCM write multiplexer comprises the inverted contents of the multiplexer that are fed back from the TCCM write buffer. These inverted inputs are used to convert binary inputs to the TCCM write multiplexer into the phase encoded (PE) format. The TCCM write multiplexer and write buffer operate together to perform this function.

The output of the write multiplexer is clocked into the write buffer. In NRZI mode, this clock occurs once for every character written on tape. In PE mode, the clock occurs twice for every character written: once when normal data is output from the write multiplexer and once again when inverted data is output from the write multiplexer. It is this operation that produces phase encoding in PE mode. Figure 4-3 shows the timing of write multiplexer-write buffer operation for PE and NRZI modes. Note that for NRZI mode the output of the write buffer is still in binary form. The output of the TCCM write buffer is then applied to signal drivers on M8937 that transmit the data to the slave bus.

In order to write tape mark (TM) characters or the IDB, appropriate codes are obtained by clearing selected bits in the slave drivers on M8937 and forcing the data lines to their desired values.

Timing for TCCM and bit fiddler write operations is derived from WRT CLK, which is generated in the slave transport and transmitted to the TM03. WRT CLK is also gated in the TM03 to produce REC pulses, which are transmitted back to the slave transport via the slave bus.

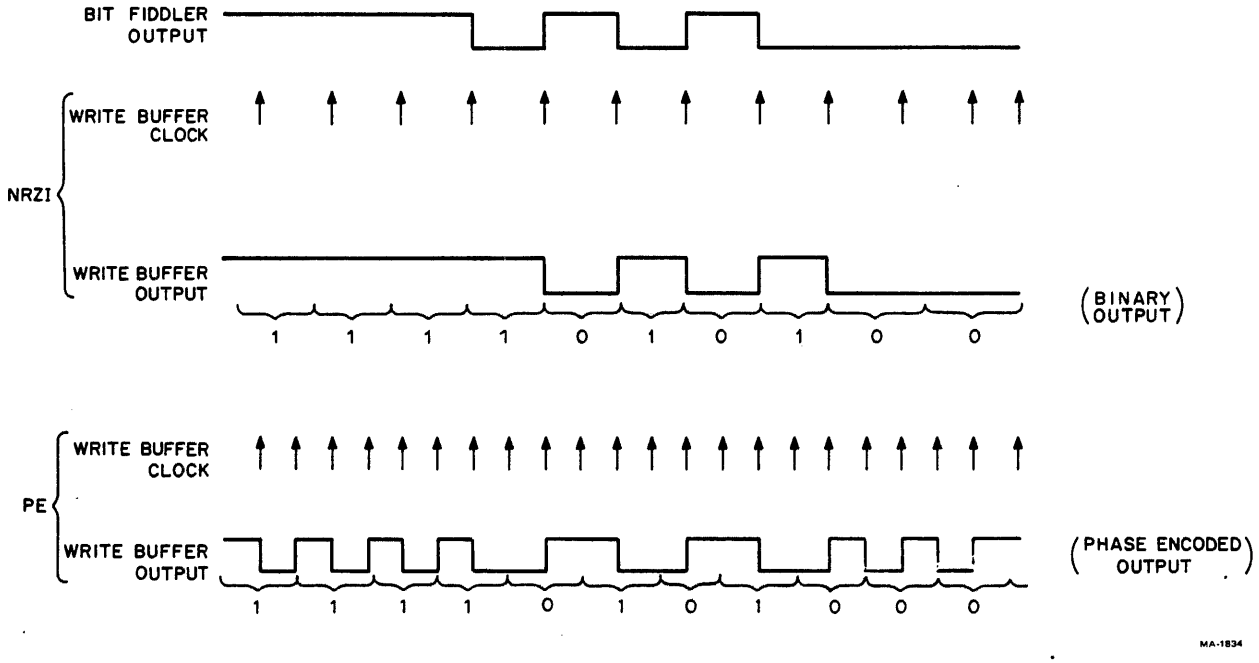


Figure 4-3 TCCM Write Timing

4.1.2 Read Data Path

The read data path, shown in the TM03 block diagram (Figure 1-7), is discussed in this section in greater detail (Figure 4-4).

Tape characters are sent from the slave transport across the slave bus read data lines to the TM03 TCCM module. The read data is passed through the TCCM read multiplexer to the three data sync (PE) modules and the tape control-NRZI module. However, the operation of one of these modules will be disabled, depending on whether the TM03 is operating in PE or NRZI mode. The mode selection is accomplished automatically by sensing the presence or absence of a PE ID burst. Once selected, the mode cannot be changed while reading that particular tape reel. This is true even though the TM03 may select another transport and then return to the original transport for another read operation.

In NRZI mode, the tape control-NRZI module is enabled, and data is strobed from the TCCM read multiplexer into the tape control-NRZI read latch by RDS (read data strobe). RDS, generated from RSDO (read strobe delay over) transmitted from the slave, occurs when a valid tape character is known to be at the output of the TCCM read multiplexer. RDS also clocks the CRCC and LRCC generator, so that the data being read off the tape can be validated at the end of the read operation by comparing the generated CRCC/LRCC against the CRCC and LRCC read off the tape. If a CRC error is detected and the error is confined to a single track, the software can implement error corrections on the data. The contents of the tape control-NRZI module are available to the maintenance register module (M8905-YB) multiplexer.

In PE mode, the tape control-NRZI circuitry is disabled while the data sync and tape control-PE modules are enabled. The phase-encoded data is input to three data sync modules (each module has three channels which process three data bits), which sync onto the frequency of the data during the preamble. The PE data on each channel is then decoded and stored in a deskew buffer (one per channel). Only when all nine bits of a character are available in the nine deskew buffers is the character read from the buffers. Because each deskew buffer has a capacity of 2×8 bits, a skew of $8 - 1 = 7$ characters can be accommodated by the TM03.

The outputs of the deskew buffers are input to error correction circuitry. If a vertical parity error occurs along with a single dead track error, the data on the dead track is corrected on the fly. The data (minus parity) is then output to the multiplexer on the maintenance register module.

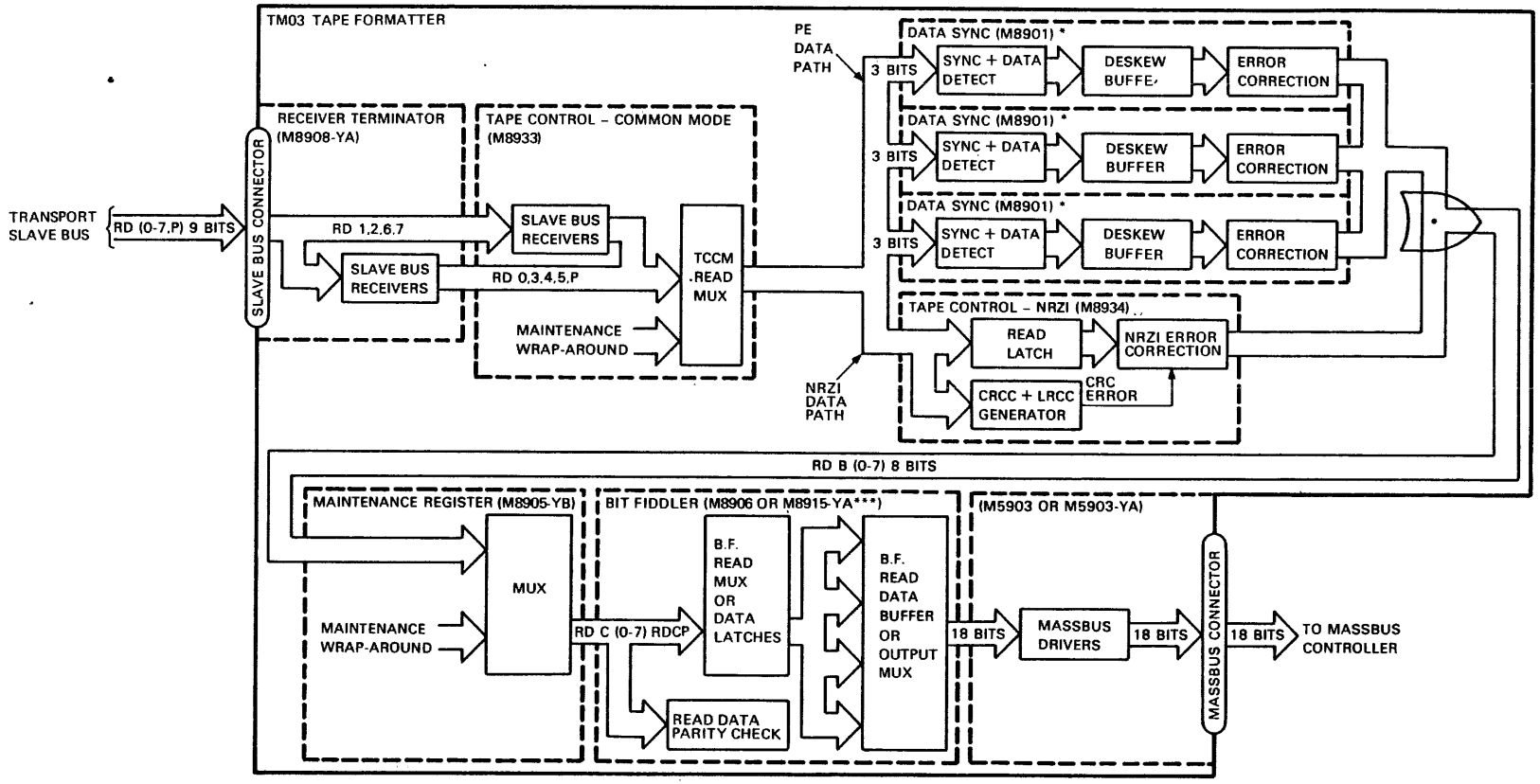
The maintenance register multiplexer passes the data character through to the bit fiddler, where vertical parity is checked on each character. The characters are then loaded into position in the bit fiddler read data buffer (or output multiplexer on M8915-YA). When the read data buffer is full (this will require two or more tape characters), the bit fiddler issues SCLK to the Massbus controller.

Read data and SCLK are driven to the Massbus controller by the Massbus drivers (M5903 or M5903-YA). When the controller receives SCLK, it strobes in the word on the data lines of the Massbus.

4.1.3 Rewind Operational Sequence

A program-controlled rewind operation may be initiated by one of two commands from the processor. One of these commands (07_8) performs the rewind operation and retains the transport on-line. The other command (03_8) places the transport off-line immediately after command initiation. Both rewind commands function identically in the TM03.

Figure 4-5 illustrates the major functional sequences of a rewind operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description.



* M8901-YB FOR 45 IPS SLAVES
M8901-YC FOR 75 IPS SLAVES
M8901-YD FOR 125 IPS SLAVES

* * M8934-YA WHEN USED WITH 75 IPS SLAVES (TU 45)

* * * MAY ALSO BE M8915 EXCEPT ON 125 IPS TRANSPORTS WHICH MUST USE M8915-YA

Figure 4-4 Read Data Path

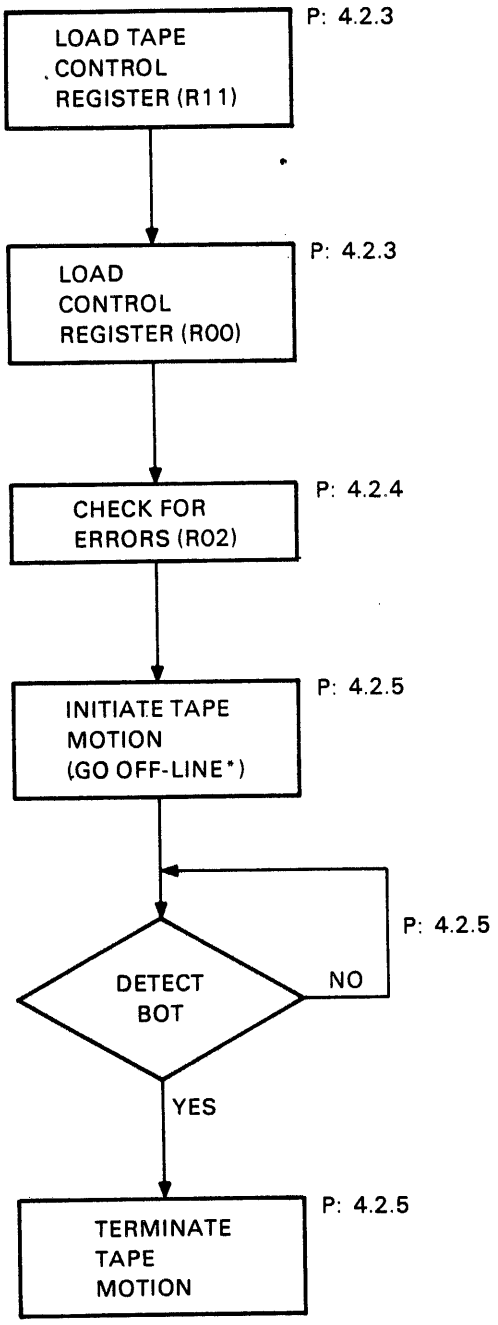


Figure 4-5 Rewind Operational Flowchart

4.1.3.1 Command Initiation – To initiate a program-controlled rewind operation, the Massbus controller first places the address code of the desired TM03 on the drive select lines of the Massbus. It then performs a register write into the tape control register (R11), selecting the slave desired to perform the rewind operation. The TM03 places the slave select bits of the tape control register on the slave bus. The Massbus controller then writes the operational function code of the rewind command (03_8 or 07_8) into the control register (R00). The TM03 decodes the function code and asserts RWND L on the slave bus. (If a rewind/off-line operation has been specified, the TM03 also asserts WRITE L.) It then checks for errors, and, if there are none, issues SLAVE SET PLS L and STOP L to the transport and clears the GO bit in the control register.

4.1.3.2 Command Execution – The selected transport executes the rewind operation independently. The Massbus controller and the TM03 can divert attention to other transports while the rewind is in progress.

4.1.3.3 Command Termination – When the transport detects the BOT marker, the rewind operation is terminated. The transport then asserts SET SSC (slave status change) on the slave bus, which causes the attention bit in the TM03 to be set. This results in ATTN H being asserted on the Massbus, thereby notifying the Massbus controller.

4.1.4 Space Operational Sequence

Figure 4-6 illustrates the major functional sequences of a space operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description.

4.1.4.1 Command Initiation – To initiate a space operation, the Massbus controller first places the address code of the desired TM03 on the drive select lines of the Massbus. It then performs a register write into the tape control register, selecting the slave transport desired to perform the space operation. The TM03 places the slave select bits of the tape control register on the slave bus.

The Massbus controller then loads the 2's complement of the number of tape records to be spaced into the TM03 frame count register. Following this, the controller loads the control register with the operational function code of the space command (31_8 for space forward, 33_8 for space reverse). The TM03 decodes the function code and asserts FWD L or REV L on the slave bus. It then checks for errors, and if there are none, issues SLAVE SET PLS and EMD to the slave transport.

4.1.4.2 Command Execution – The transport, which is enabled by its address code on the slave select lines (SS0–2), responds to SLAVE SET PLS by initiating tape motion (forward or reverse).

The selected transport also responds to EMD by multiplexing motion delay presets onto the read data lines of the slave bus. The TM03 uses the presets to generate a motion delay, at the end of which the read capability of the transport is enabled. (As the tape moves under the read heads, tape characters are detected as during a read operation; however, bit fiddler operation is suppressed.)

When the end of the record, i.e., IRG (interrecord gap), is detected, a signal (RECORD H) from the TCCM module increments the frame count register, and another motion delay is generated. At the end of this motion delay, STOP L is asserted on the slave bus and causes the transport to begin the motion termination sequence. Soon after, however, another SLAVE SET PLS from the TM03 reinitiates tape motion and another motion delay is generated. At the end of this motion delay, the read heads will detect the next record. At the end of this record, the frame count register is again incremented and another motion delay occurs. This sequence continues for all the records spaced. The SLAVE SET PLS reinitiates tape motion before the tape actually starts to slow down. Thus the space operation continues at a constant speed.

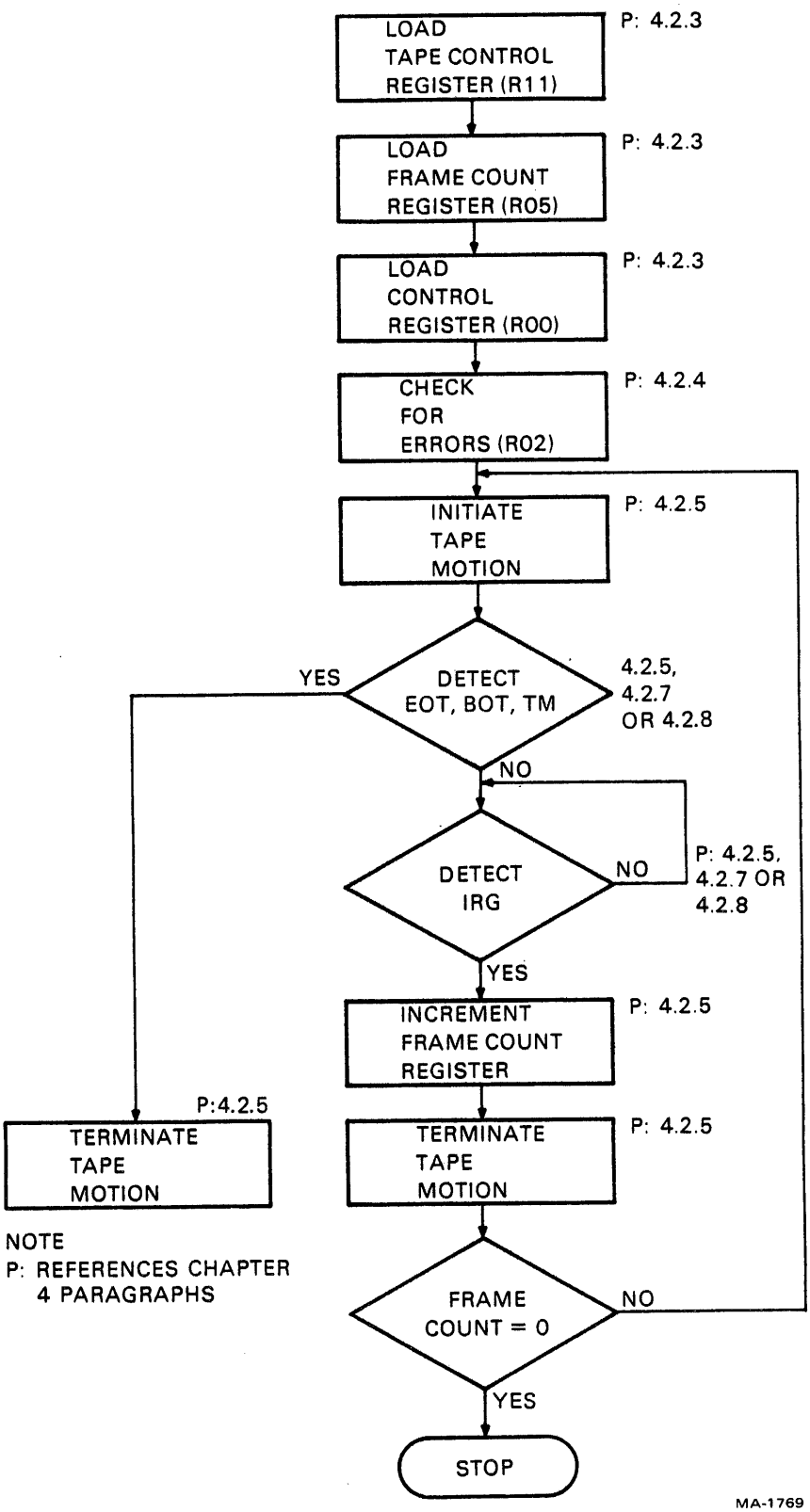


Figure 4-6 Space Operational Flowchart

4.1.4.3 Command Termination – After the last record has been spaced, the frame count register will overflow to zero. This will inhibit SLAVE SET PLS to the transport and tape motion will be terminated. If BOT, EOT, or TM are detected before the frame count register overflows, tape motion will also be terminated. Upon detection of BOT, EOT, TM, or frame count overflow, the GO bit of the control register is cleared.

4.1.5 Erase Operational Sequence

Figure 4-7 illustrates the major functional sequences of an erase operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description.

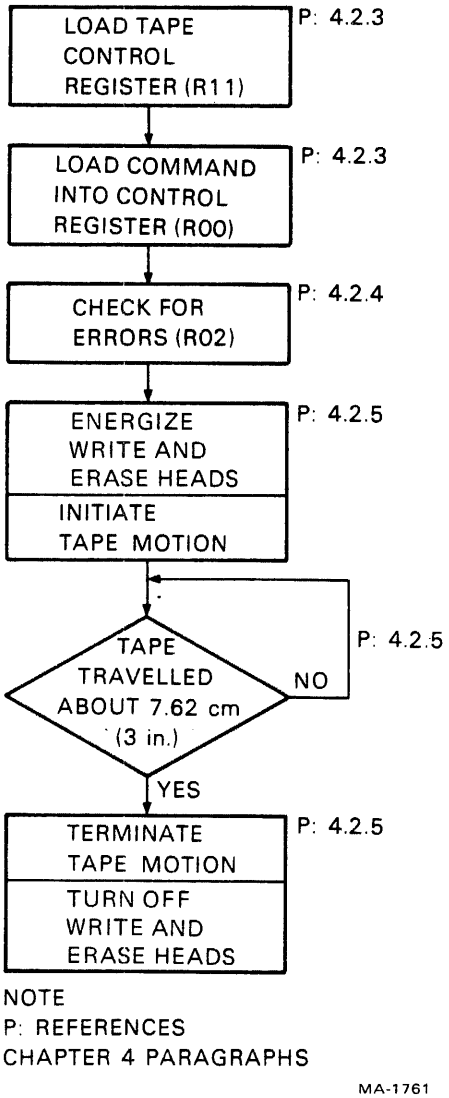


Figure 4-7 Erase Operational Flowchart

4.1.5.1 Command Initiation – To initiate an erase operation, the Massbus controller first places the address code of the desired TM03 on the drive select lines of the Massbus. It then performs a register write into the tape control register, selecting the slave transport desired to perform the erase operation. The TM03 places the slave select bits of the tape control register on the slave bus. The Massbus controller then loads the TM03 control register with the operational function code (25_8) of the erase command. The TM03 decodes the function code and asserts FWD L and WRITE L on the slave bus. It then checks for errors, and, if there are none, issues SLAVE SET PLS and EMD (enable motion delay) to the slave transport.

4.1.5.2 Command Execution – The transport which is enabled by its address code on the slave select lines, responds to SLAVE SET PLS by initiating forward tape motion. It also responds to EMD by gating out a motion delay preset onto the slave bus read data lines. The preset is loaded into a counter in the TCCM module, which is then counted up. When a count of 2^{14} is reached, the motion delay has expired and tape motion is considered to be up to speed. The transport then executes the erase operation.

4.1.5.3 Command Termination – When the start motion delay is over, another motion delay is started. At the end of this second (stop) motion delay, the TM03 asserts STOP L on the slave bus. STOP L causes the GO bit of the control register to be cleared.

4.1.6 PE Data Read Operational Sequence

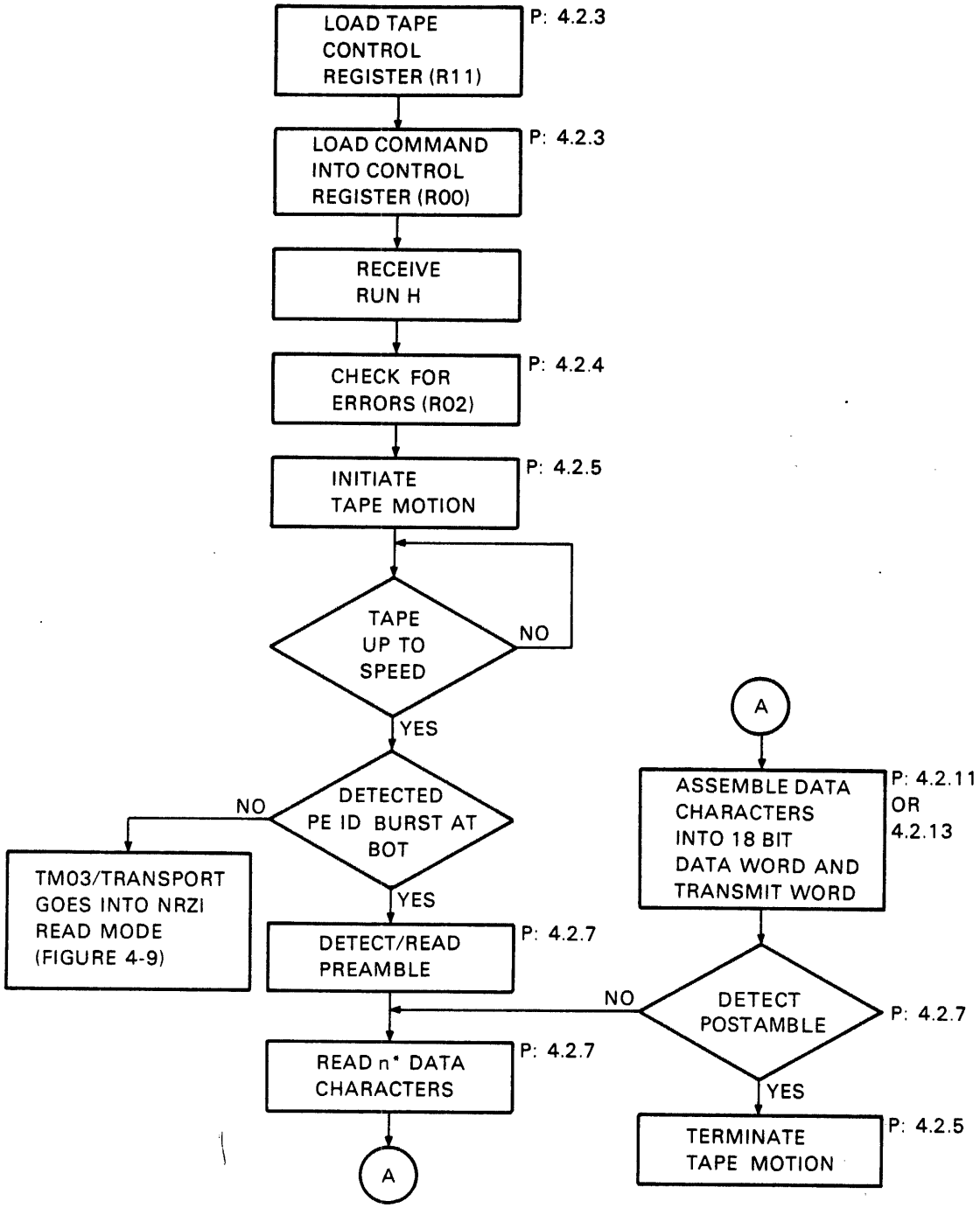
Figure 4-8 illustrates the major functional sequences of a PE read operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description.

4.1.6.1 Command Initiation – To initiate a PE read operation, the Massbus controller first places the address code of the desired TM03 on the drive select lines of the Massbus. It then performs a register write into the tape control register, specifying the selected slave transport and the tape character format.

The TM03 places the slave select (SS0–2) bits of the tape control register on the slave bus. The Massbus controller then loads the TM03 control register with the operational function code of a read operation (71_8, read forward; 77_8, read reverse; 51_8, write check forward; or 57_8, write check reverse) and asserts RUN on the Massbus. The TM03 decodes the function code and asserts FWD L or REV L on the slave bus. It then checks for errors, and, if there are none, asserts OCC on the Massbus to notify the controller and other drives that it is occupying the data bus of the Massbus. The TM03 then transmits SLAVE SET PLS to the slave transport and initiates a motion delay.

4.1.6.2 Command Execution – The slave transport, which is enabled by its address code on the slave select lines (SS0–2) of the slave bus, responds to SLAVE SET PLS by initiating tape motion (forward or reverse).

The TM03 always starts to read a tape from BOT in the PE mode. After the tape is up to speed, the TM03 looks for the PE ID burst. After finding the burst, the TM03/transport is locked into the 1600 bits/in PE mode for the entire tape. If the TM03 selects another transport and then returns to this transport to continue the read operation, the PE mode will be automatically implemented.



NOTE
P: REFERENCES
CHAPTER 4 PARAGRAPHS

*n DEPENDS ON SELECTED FORMAT

MA-1756

Figure 4-8 PE Read Operational Flowchart

The TM03 PE read circuits then read the record preamble which is followed by the data characters. These are deskewed in the data sync (M8901)* and tape control-PE (M8932) logic, and sent to the bit fiddler (via the maintenance register module), which assembles the characters into 16- or 18-bit data words and places them on the data bus. When a data word is assembled, the bit fiddler notifies the Massbus controller, which then strobes the word from the data bus. The bit fiddler continues this assembly of data characters into 16- or 18-bit words until the first character of the postamble is detected.

4.1.6.3 Command Termination – The TM03 reads the postamble, which signifies the end of the record, and asserts EBL H (end of block) on the Massbus. When the postamble has been read, a motion delay sequence is initiated, at the end of which STOP L is asserted on the slave bus. STOP L terminates tape motion in the slave transport. It also clears the GO bit in the control register, which causes OCC to be negated on the Massbus.

4.1.7 NRZI Data Read Operational Sequence

Figure 4-9 illustrates the major functional sequences of an NRZI read operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description.

4.1.7.1 Command Initiation – To initiate an NRZI read operation, the Massbus controller first places the address code of the desired TM03 on the drive select lines of the Massbus. It then performs a register write into the tape control register, specifying selected slave transport and tape character format. The TM03 places the slave select (SS0–2) bits of the tape control register on the slave bus. The Massbus controller then loads the TM03 control register with the operational function code of a read operation (71_8, read forward; 77_8, read reverse; 51_8, write check forward; or 57_8, write check reverse) and asserts RUN H on the Massbus. The TM03 decodes the function code and asserts FWD L or REV L on the slave bus. It then checks for errors, and, if there are none, asserts OCC on the Massbus to notify the controller and other drives that it is occupying the data bus of the Massbus. The TM03 then transmits SLAVE SET PLS to the slave transport to initiate a motion delay.

4.1.7.2 Command Execution – The slave transport, which is enabled by its address code on the slave select lines (SS0–2) of the slave bus, responds to SLAVE SET PLS by initiating tape motion (forward or reverse). When the motion delay has timed out, the tape is assumed to be up to speed; the TM03 then negates ACCL L on the slave bus and the transport starts to read data. The TM03 always starts to read a tape from BOT in the PE mode. It looks for a PE ID burst, and, if it does not find one, switches into the 800 bits/in NRZI mode. The TM03/transport then becomes locked into this mode for the entire tape. If the TM03 selects another transport and then returns to this transport to continue the read operation, the NRZI mode will be automatically implemented.

When tape characters are detected by the transport, they are transmitted via the slave bus to the TCCM module. Along with each tape character, the transport issues an RSDO (read strobe delay over) pulse, via the slave bus, to the tape control-NRZI module. RSDO pulses cause the tape control-NRZI module to strobe the tape characters into the TCCM module from the slave bus. The characters then pass to the read latch in the tape control-NRZI module. The characters are now available to the bit fiddler. LRCC and CRCC are generated from the data as it passes through the tape control-NRZI module. These will be used later to check the validity of the data read.

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*M8901-YB for 114.3 cm/s (45 in/s) slaves.
M8901-YC for 190.5 cm/s (75 in/s) slaves.
M8901-YD for 317.5 cm/s (125 in/s) slaves.

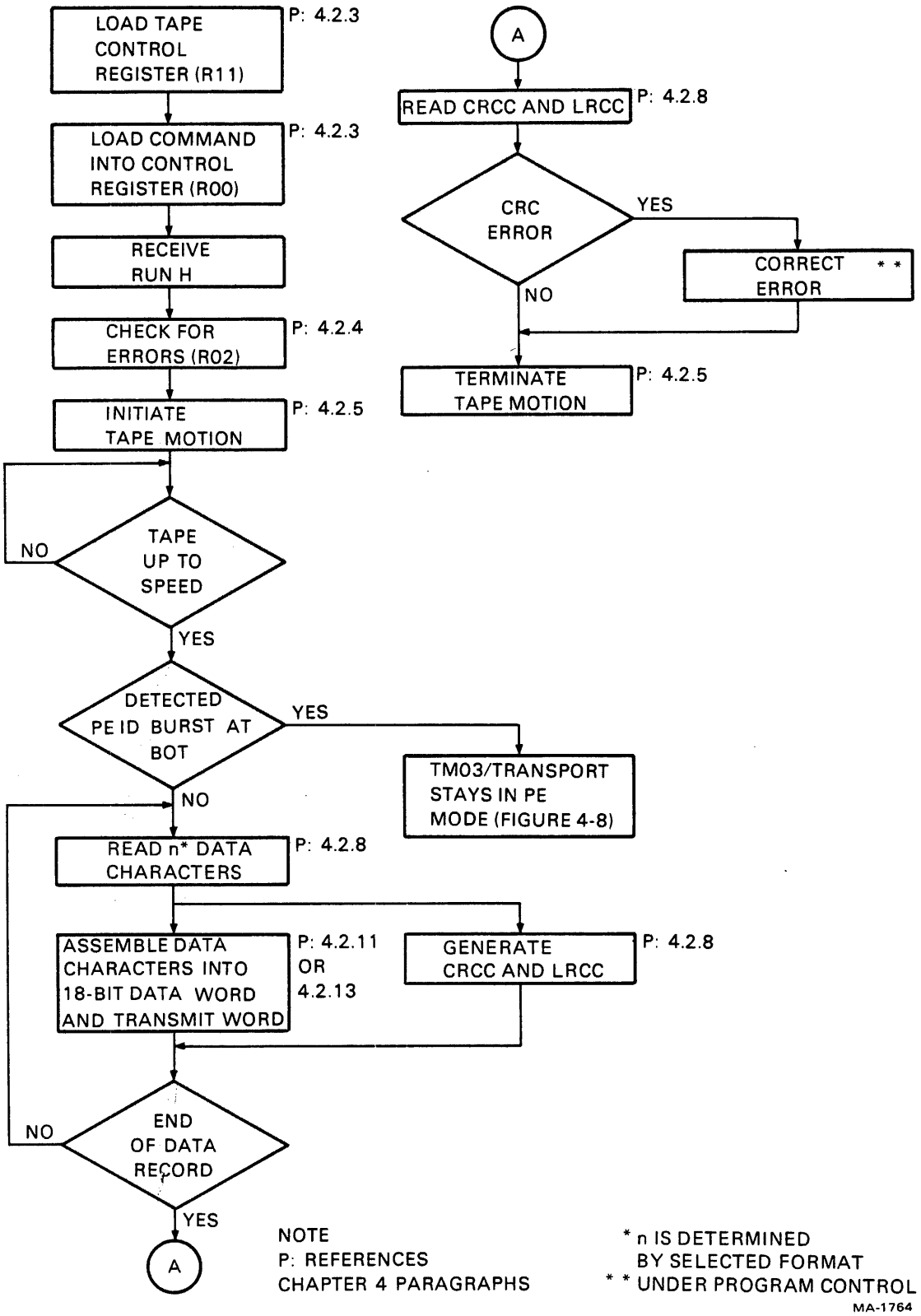


Figure 4-9 NRZI Read (Forward) Operational Flowchart

The bit fiddler assembles the characters into 16- or 18-bit data words and places them on the data bus. When a data word is assembled, the bit fiddler notifies the Massbus controller, which then strobes in the word from the data bus. The bit fiddler continues this assembly of data characters into 16- or 18-bit words until the end of the data record.

At the end of the data record (read in the forward direction), the read logic (less the bit fiddler) continues its operation, reading the CRCC and strobing it into the check character register, and then reading the LRCC. Discrepancies between generated CRCC/LRCC and detected CRCC/LRCC cause their respective error bits to be set. If a CRC error is detected, the program can re-read the record and correct the error if it is confined to a single track.

During a reverse read, the LRCC character is encountered first at the start of the read operation, but is ignored. The CRCC is encountered next, and strobed into the check character register. At the end of the record, a CRC is performed. If an error is detected, the program may perform a forward read of the faulty record and accomplish error correction as described in the preceding paragraph. No LRC error is generated during a reverse read. The assembly of characters into data words will differ when reading in the reverse direction, depending on the data format selected.

4.1.7.3 Command Termination – When the data and LRCC/CRCC have been read, the transport read heads will encounter the IRG. The absence of tape characters causes a motion delay, at the end of which STOP L is asserted on the slave bus and EBL (end of block) is asserted on the Massbus. STOP L terminates tape motion in the transport. It also clears the GO bit in the control register, which causes OCC to be negated on the Massbus.

4.1.8 PE Data Write Operational Sequence

Figure 4-10 illustrates the major functional sequences of a PE data write operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description.

4.1.8.1 Command Initiation – To initiate a PE write operation, the Massbus controller first places the address code of the desired TM03 on the drive select lines of the Massbus. It then performs a register write into the tape control register, specifying selected slave transport, tape character format, and tape data density (PE = 1600 bits/in). The TM03 places the slave select (SS0–2) and density (DEN0–2) bits of the tape control register on the slave bus. The Massbus controller then loads the 2's complement of the number of tape characters to be written into the TM03 frame count register. Following this, the controller loads the control register with the operational function code (61_8) of the write forward command. The TM03 decodes the function code and asserts FWD L and WRITE L on the slave bus. It then checks for errors, and, if there are none, asserts OCC on the Massbus to notify the controller and other drives that it is occupying the data bus of the Massbus.

When the controller has data available for transfer, it asserts RUN H on the Massbus. The TM03 responds by asserting SLAVE SET PLS on the slave bus to start tape motion, and by accepting the first data word from the controller.

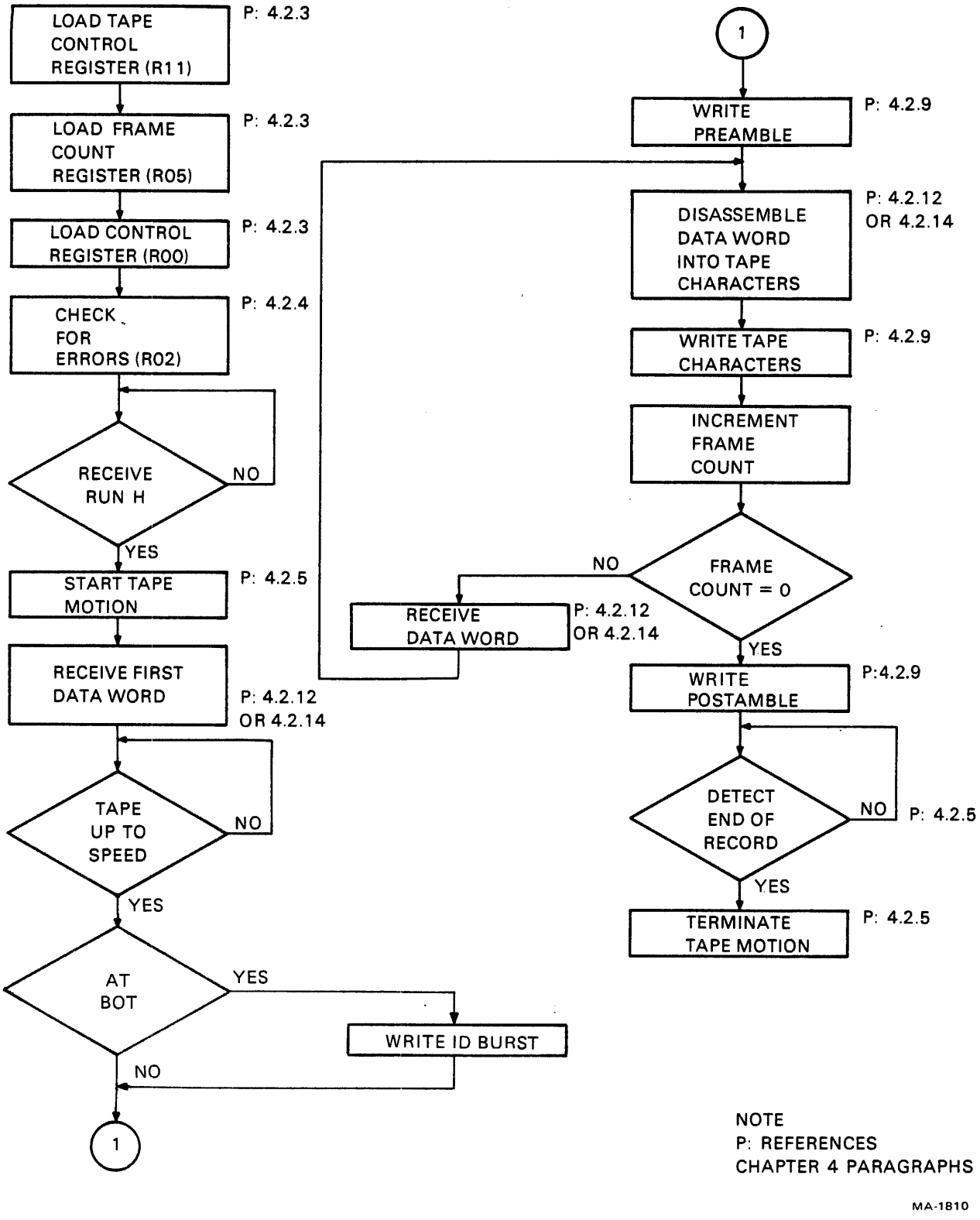


Figure 4-10 PE Data Write Operational Flowchart

4.1.8.2 Command Execution – The transport, which is enabled by its address code on the slave select lines (SS0–2) of the slave bus, responds to SLAVE SET PLS by initiating forward tape motion.

After a motion delay, the TM03 negates ACCL L on the slave bus. This notifies the slave transport that it is up to speed. If the tape is starting from BOT, an ID burst is written at this point. The negation of ACCL L allows the slave transport to transmit WRT CLK to the TM03. Upon receipt of WRT CLK, the TM03 begins generating a preamble. When the preamble (forty all-0s characters and one all-1s character) has been written, the bit fiddler begins disassembling the first data word into tape characters. When it has disassembled the first data word, it requests the next data word from the Massbus controller, and continues to do so until all the data words have been transferred. Each time the bit fiddler generates a character, the frame count register is incremented and a vertical parity bit is generated. The tape character is converted to PE format and transmitted to the write logic of the slave transport. When the frame count register overflows to zero, the TM03 asserts EBL (end of block) to the controller and generates a postamble which is written on tape.

Writing the first record of a tape in the 1600 bits/in PE mode locks the TM03/transport into the PE mode insofar as that tape is concerned. The mode cannot be changed at some later point on the tape. If the TM03 selects another transport and then returns to this transport to continue the write operation, the PE mode will be automatically implemented.

4.1.8.3 Command Termination – While the PE write command is being executed, the read logic in the transport and in the TM03 is enabled and reads the record being written. When the TM03 read circuitry detects the end of the record, a motion delay is generated at the end of which the TM03 asserts STOP L on the slave bus, thereby terminating tape motion. STOP L also clears the GO bit of the control register, which causes OCC to be negated.

4.1.9 NRZI Data Write Operational Sequence

Figure 4-11 illustrates the major functional sequences of an NRZI data write operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description.

4.1.9.1 Command Initiation – To initiate an NRZI write operation, the Massbus controller first places the address code of the desired TM03 on the drive select lines of the Massbus. It then performs a register write into the tape control register, specifying selected slave transport, tape character format, and tape data density. The TM03 places the slave select (SS0–2) and density (DEN0–2) bits of the tape control register on the slave bus. The Massbus controller then loads the 2s complement of the number of tape characters to be written into the TM03 frame count register. Following this, the controller loads the control register with the operational function code (61_8) of the write forward command. The TM03 decodes the function code and asserts FWD L and WRITE L on the slave bus. It then checks for errors, and, if there are none, asserts OCC on the Massbus to notify the controller and other drives that it is occupying the data bus of the Massbus.

When the controller has data available for transfer, it asserts RUN H on the Massbus. The TM03 responds by asserting SLAVE SET PLS on the slave bus to start tape motion, and by accepting the first data word from the controller.

4.1.9.2 Command Execution – The slave transport, which is enabled by its address code on the slave select lines (SS0–2) of the slave bus, responds to SLAVE SET PLS by initiating forward tape motion. After a motion delay, the TM03 negates ACCL L on the slave bus. This notifies the slave transport that it is up to speed, and enables it to transmit WRT CLK to the TM03.

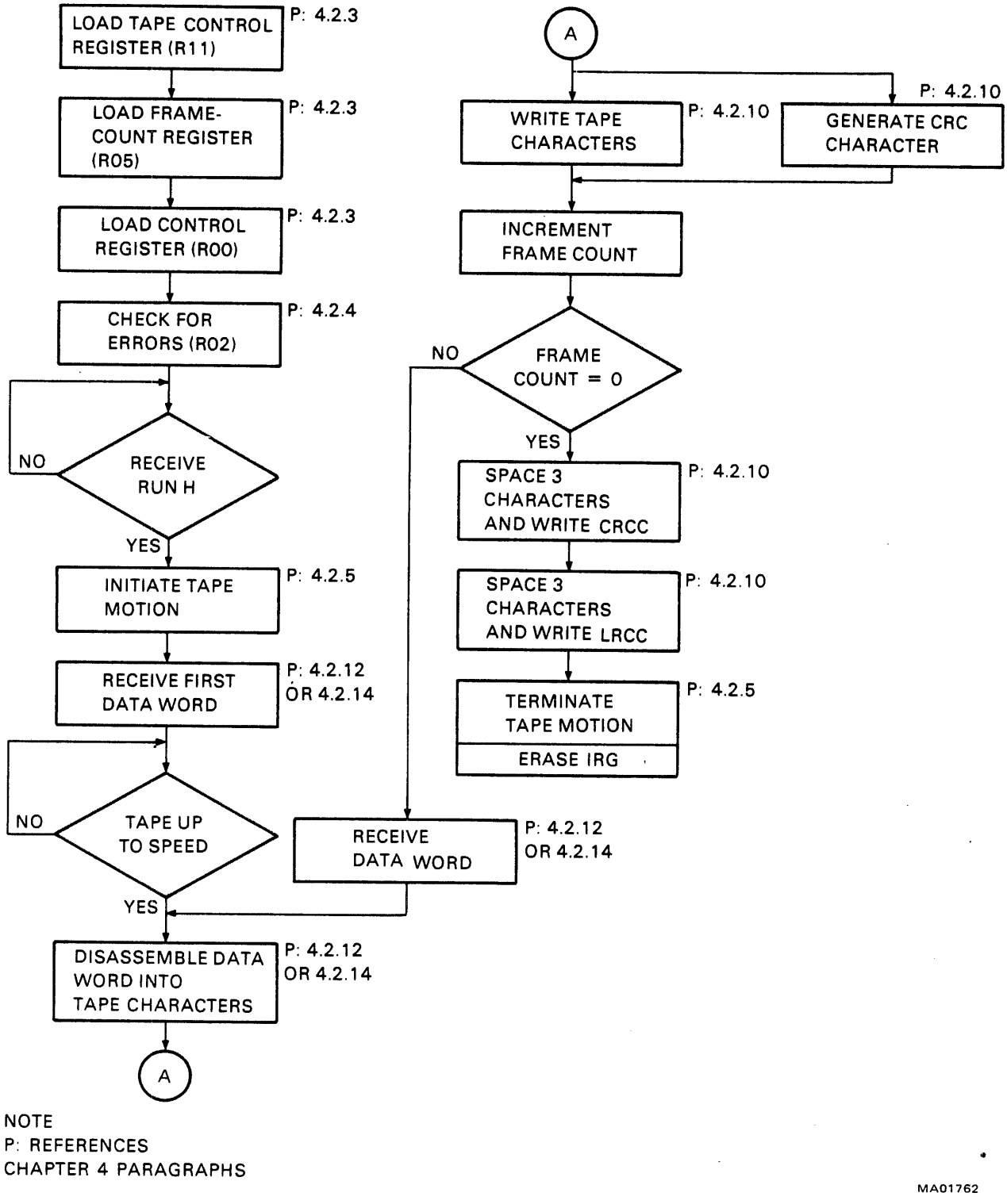


Figure 4-11 NRZI Data Write Operational Flowchart

Upon receipt of WRT CLK by the TM03, the bit fiddler begins disassembling the first data word into characters. When it has disassembled the first data word, it requests the next data word from the Massbus controller, and continues to do so until all the data words have been transferred. Each time the bit fiddler generates a character, the frame count register is incremented, a vertical parity bit is generated, the CRC generator is updated, and the tape character is transmitted to the write circuitry of the slave transport. When the frame count register overflows to zero, the TM03 transmits EBL (end of block) to the controller. It then generates the timing to write the generated CRCC and the LRCC.

Writing the first record of a tape in the 800 bits/in NRZI mode locks the TM03/transport into the NRZI mode insofar as that tape is concerned. The mode of writing cannot be changed at some later point on the tape. If the TM03 selects another transport and then returns to this transport to continue the write operation, the NRZI mode will be automatically implemented.

4.1.9.3 Command Termination – While the NRZI write command is being executed, the read logic in the transport and in the TM03 is enabled and reads the record being written. When the TM03 read circuity detects the end of the record, a motion delay is generated at the end of which the TM03 asserts STOP L on the slave bus, thereby terminating tape motion. STOP L also clears the GO bit of the control register, which causes OCC to be negated.

4.1.10 Write Tape Mark Operational Sequence

The tape mark is a special tape record used to separate data on tape. Although a write tape mark command may be issued at any time, the most common use of this command is as a "software bookmark" to designate the end of a group of related records. It is possible to quickly locate the beginning of a group of related data records by searching the tape for written tape marks. This is accomplished by loading the frame count register with a record count larger than the number of records in any existing group of records, and then issuing a space command. The transport will space to the tape mark and terminate motion despite the fact that frame count overflow does not occur.

Figure 4-12 illustrates the major functional sequences of a write tape mark operation and the following paragraphs describe this operation in slightly greater depth. Each functional box on the flowchart is referenced to an applicable detailed logic description.

4.1.10.1 Command Initiation – To initiate a write tape mark operation, the Massbus controller first places the address code of the desired TM03 on the drive select lines of the Massbus. It then performs a register write into the tape control register, selecting the slave transport desired to perform the write tape mark operation and the mode (density) in which the tape mark characters are to be written. The TM03 places the slave select (SS0–2) and density (DEN0–2) bits of the tape control register on the slave bus.

The Massbus controller then loads the TM03 control register with the operational function code (27_8) of the write tape mark command. The TM03 decodes the function code and asserts FWD L and WRITE L on the slave bus. It then checks for errors, and, if there are none, issues SLAVE SET PLS to the slave transport and generates a motion delay.

4.1.10.2 Command Execution – The slave transport, which is enabled by its address code on the slave select lines, responds to SLAVE SET PLS by initiating tape motion. When the motion delay is over and the tape is up to speed, the TCCM module generates the tape mark. If the TM03 is operating in PE mode, slave bus write lines WD3, 4, and 6 are forced low, while PE 0s are generated for WD0, 1, 2, 5, 7, and P. At the same time, record pulses ($40 \times 2 = 80$) are transmitted to the transport. This results in forty 0s being written in physical tracks 1, 2, 4, 5, 7 and 8, and erasure of the remaining tracks (3, 6, 9). If the TM03 is operating in NRZI mode, the tape mark character (23_8) is forced onto the slave bus WD lines, and a record pulse is transmitted to the transport. The transport is then allowed to erase seven character lengths of tape, at which time it receives LRC STROBE on the slave bus and writes an LRCC (which will be the same as the tape mark character).

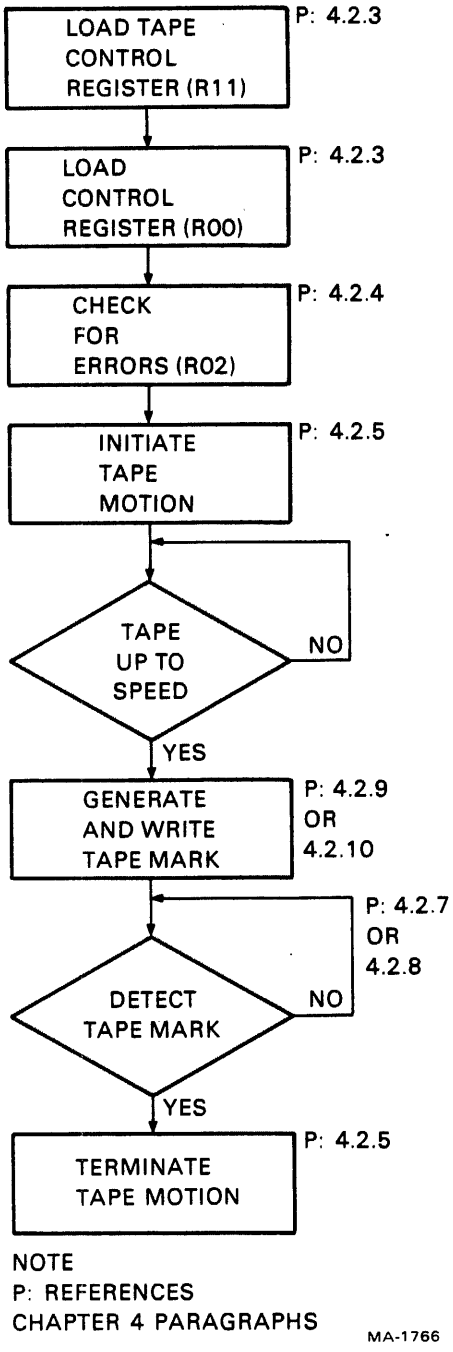


Figure 4-12 Write Tape Mark Operational Flowchart

4.1.10.3 Command Termination – While the write tape mark command is being executed, the read logic in the transport and in the TM03 is enabled and reads the tape mark being written. When the read circuitry has detected the written tape mark, a motion delay is generated by the TM03, at the end of which STOP L is transmitted to the transport. STOP L terminates tape motion and resets the GO bit in the TM03 control register.

4.2 FUNCTIONAL DESCRIPTIONS

4.2.1 Maintenance Modes

The maintenance register (R3) facilitates on-line diagnostic testing of the TM03 and allows testing of the TM03 data paths and error discrimination circuitry. A discussion of the maintenance register bits and their function follows.

1. Bit 0, Maintenance Mode (MM) – Must be loaded set when any maintenance mode function is desired.

2. Bits 1 to 4, Maintenance Op Code (MOP 0–3) – These four bits determine the maintenance function that will occur if the MM bit is set and the TM03 is loaded with the appropriate command. The op codes that are implemented are:

   a. 0000 (Null code)

   b. 0001 (Interchange Read, IRD) – In NRZI mode, causes a more stringent skew check to be made on data during read or write check operations. In PE mode, suppresses on-the-fly correction of data errors.

   c. 0010 (Even Parity) – Causes even parity to be used on the control lines of the Massbus.

   d. 0011 (Global Data Wrap-Around, WRP0) – Configures the TM03 data paths as shown in Figure 4-13. This causes a write data command to be executed as follows. Data is brought in on the data lines, divided into bytes using the algorithm defined by the format code resident in the tape control register, formatted as either NRZI or PE write data, multiplexed into the read circuitry, and deposited in the maintenance register data field.

   e. 1100 (Global Data Wrap-Around NRZI Error Correction, WRP4) – Performs the same function as the global wrap-around (code = 0011) with the exception that the write CRC generator will not be clocked in NRZI mode. The purpose of this wrap-around is to allow the generation of CRC errors during maintenance mode testing to enable CRC error correction sequencing.

   f. 0100 (Partial Data Wrap-Around, WRP1) – Configures the TM03 data path as shown in Figure 4-14. This causes a write data command to be executed as follows: data is brought in on the data lines, divided into bytes using the algorithm defined by the format code resident in the tape control register, formatted as either NRZI or PE write data, and deposited in the maintenance register data field.

   g. 0101 (Formatter Write Data Wrap-Around, WRP2) – Configures the TM03 data path as shown in Figure 4-15. This causes a write data command to be executed as follows. Data is brought in on the data lines, divided into bytes using the algorithm defined by the format code resident in the tape control register, and deposited in the maintenance register data field.

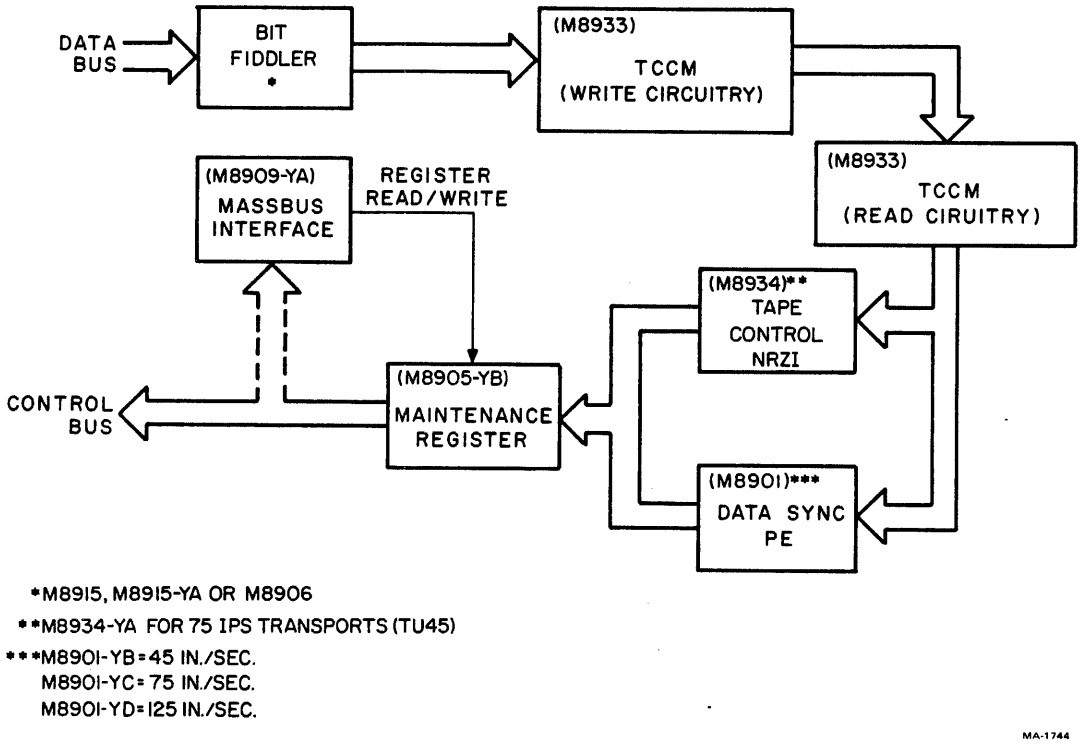


Figure 4-13 Global Wrap-Around (WRP0 and WRP4)

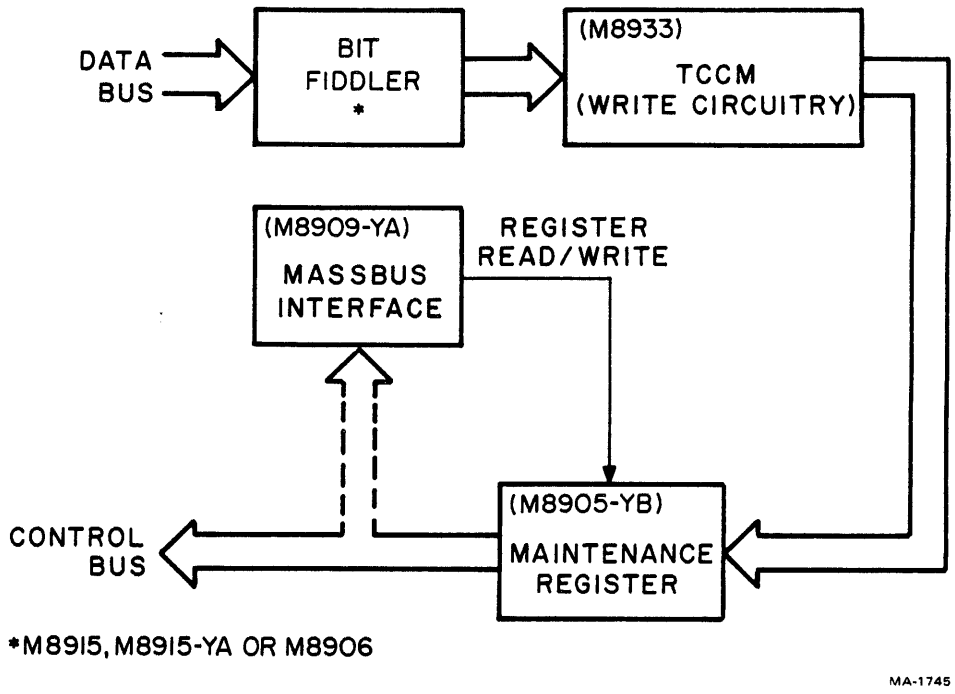


Figure 4-14 Partial Wrap-Around (WRP1)

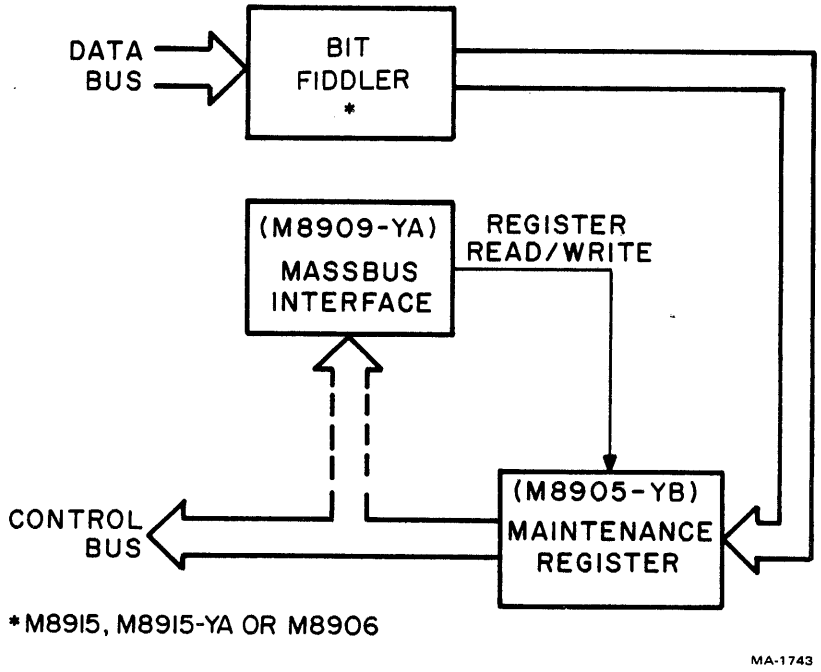


Figure 4-15 Formatter Write Wrap-Around (WRP2)

h. 0110 (Formatter Read Data Wrap-Around, WRP3) – Configures the TM03 data path as shown in Figure 4-16. This causes a read data command to be executed as follows. Data is taken from the maintenance register data field, multiplexed into the formatting logic byte by byte, formed into data bus words using the algorithm defined by the format code resident in the tape control register, and transmitted to the controller.

   In addition, the op code suppresses reception of the Massbus WCLK signal. Thus, an attempt to perform a write operation with this op code in the maintenance register will result in detection of DTE.

i. 0111 (Cripple Reception of OCC) – An attempt to perform any data transfer operation with this op code in the maintenance register will result in detection of DTE.

j. 1000 (Illegal Check Character, ILCC) – In NRZI mode, suppresses initialization of the CRC logic, resulting in CRC errors. In PE mode, suppresses detection of data in logical track 1.

k. 1001 (Incorrect Tape Mark) – Causes bit 5 of tape data bytes to remain in the negated state. In PE mode, suppresses detection of data in logical tracks 1 and 2.

l. 1010 (Maintenance Mode End of Record, MMEOR) – Used to signal the end of a maintenance mode operation, thus causing the GO bit to become negated.

m. 1011 (Incorrect Preamble, INC PREAMBLE) – Causes logical bit 1 of a PE preamble and postamble to be inverted during a write data command, resulting in generation of invalid preambles and postambles.

3. Bit 5, Maintenance Mode Clock (MC) – This bit controls the sequencing of data through the TM03 data paths when operating in a maintenance mode.

4. Bit 6, Tape Speed Clock (SWC2) – This bit displays a clock signal which is obtained from the selected slave. The frequency of this clock depends on the read/write speed of the selected slave. For a 114.3 cm/s (45 in/s) transport, the frequency is the 200 bits/in rate (9 kHz); for 190.5 cm/s (75 in/s) and 317.5 cm/s (125 in/s) transports, the frequency is 7.5 kHz and 6.25 kHz, respectively (Table 4-3). This clock is displayed to aid in monitoring drive functions during maintenance mode read operations.

5. Bits 7 to 15, Maintenance Data Field (MDF 0–8) – These bits act as buffers for data generated during checks of the TM03 data paths.

Proper operation of the formatter wrap-around tests depends on three signals from the slave transport: CLOCK (SB) L, MOL (SB) L, and WRT CLK (SB) L. Also, any fault which causes incorrect RSDO pulses will interfere with wrap-around tests. Verify the status of these signals before doing extensive troubleshooting in the TM03.

4.2.2 TM03 Clocks

All clocks used in the TM03 are developed from two clock signals generated in the selected slave transport and transmitted to the TM03 over the slave bus. These two clock signals are CLOCK (SB) and WRT CLK (SB).

4.2.2.1 Clock (SB) – The frequency of CLOCK (SB) is a function of tape speed [144 kHz for 114.3 cm/s (45 in/s) slaves; 240 kHz for 190.5 cm/s (75 in/s) slaves; 400 kHz for 317.5 cm/s (125 in/s) slaves]. CLOCK (SB) is transmitted to the TM03 by an on-line, selected transport loaded with tape.

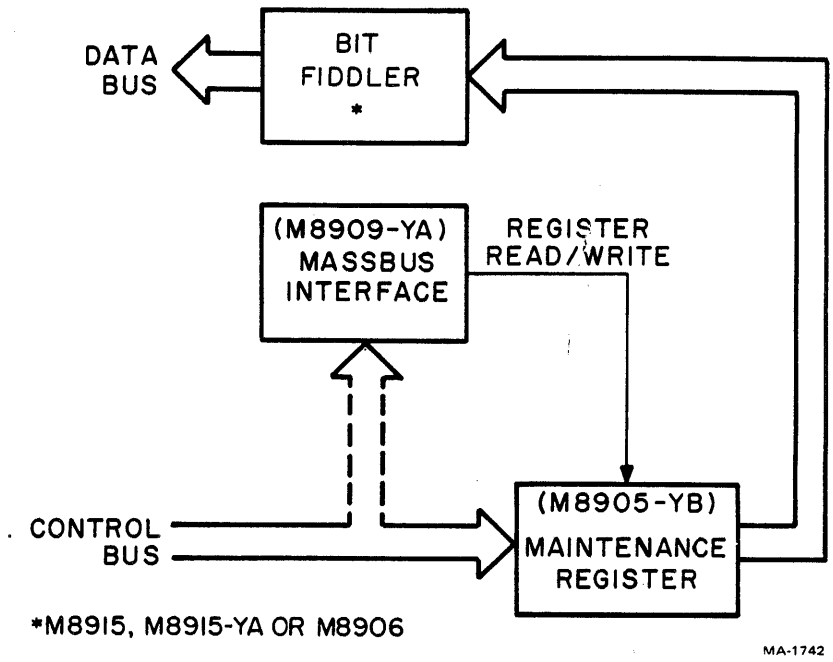


Figure 4-16 Formatter Read Wrap-Around (WRP3)

On the tape control common mode (TCCM) module (M8933), the CLOCK (SB) signal is divided to provide:

DATA HALF
800 BPI CLK
200 BPI CLK

These three clocks perform various housekeeping functions in the TM03. For example, 800 BPI CLK clocks the motion delay counter (TCCM3), and 200 BPI CLK counts the IDB counter, write end counter, and shutdown counter. DATA HALF is used in functions pertaining to PE mode. For instance, it clocks the character counter on the tape control PE module (TCPE4).

4.2.2.2 WRT CLK (SB) – The TM03 is capable of writing data at two bit densities. A separate clock signal (WRT CLK), whose frequency depends on the tape data density and on the tape speed, must be developed. WRT CLK is transmitted to the TM03 by a selected, powered slave transport, loaded with tape and running at speed (except during a rewind). It is used in the TM03 to produce the following clock signals:

WB CLK	Clocks the TCCM write buffer (TCCM2)
ST CLK	Used to generate PE write data states in the tape control-PE module (TCPE2).
PE CLK	Used in PE mode to control TCCM write multiplexing (TCCM2).

Table 4-3 lists the signal frequencies for the various TM03 clocks.

Table 4-3 TM03 Clock Signal Frequencies

Signal	114.3 cm/s Slaves (45 in/s) (TE16)	190.5 cm/s Slaves (75 in/s) (TU45)	317 cm/s Slaves (125 in/s) (TU77)
WRT CLK (NRZI)	36 kHz	60 kHz	100 kHz
WRT CLK (PE)	144 kHz	240 kHz	400 kHz
CLOCK	144 kHz	240 kHz	400 kHz
DATA HALF	72 kHz	120 kHz	200 kHz
800 BPI CLK	36 kHz	60 kHz	100 kHz
200 BPI CLK	9 kHz	15 kHz	25 kHz
TAPE SPEED CLOCK	9 kHz	7.5 kHz	6.25 kHz

4.2.3 Register Reading and Writing

The Massbus controller performs register transfers to control and determine the status of the TM03 and the slave transport. These register transfers are performed on the control bus of the Massbus.

4.2.3.1 Register Write – The Massbus controller writes into TM03 registers to control transport/TM03 operations. To accomplish a register write (Figures 4-17, 4-18 and 4-21), the controller simultaneously:

1. Places a 3-bit address code on the drive select lines
2. Places the 5-bit register select code of the desired register on the register select lines
3. Places the information to be written on the control lines
4. Places a parity bit (odd parity) on the CPA line. This parity bit is associated with the data on the control lines.
5. Asserts CTOD H.

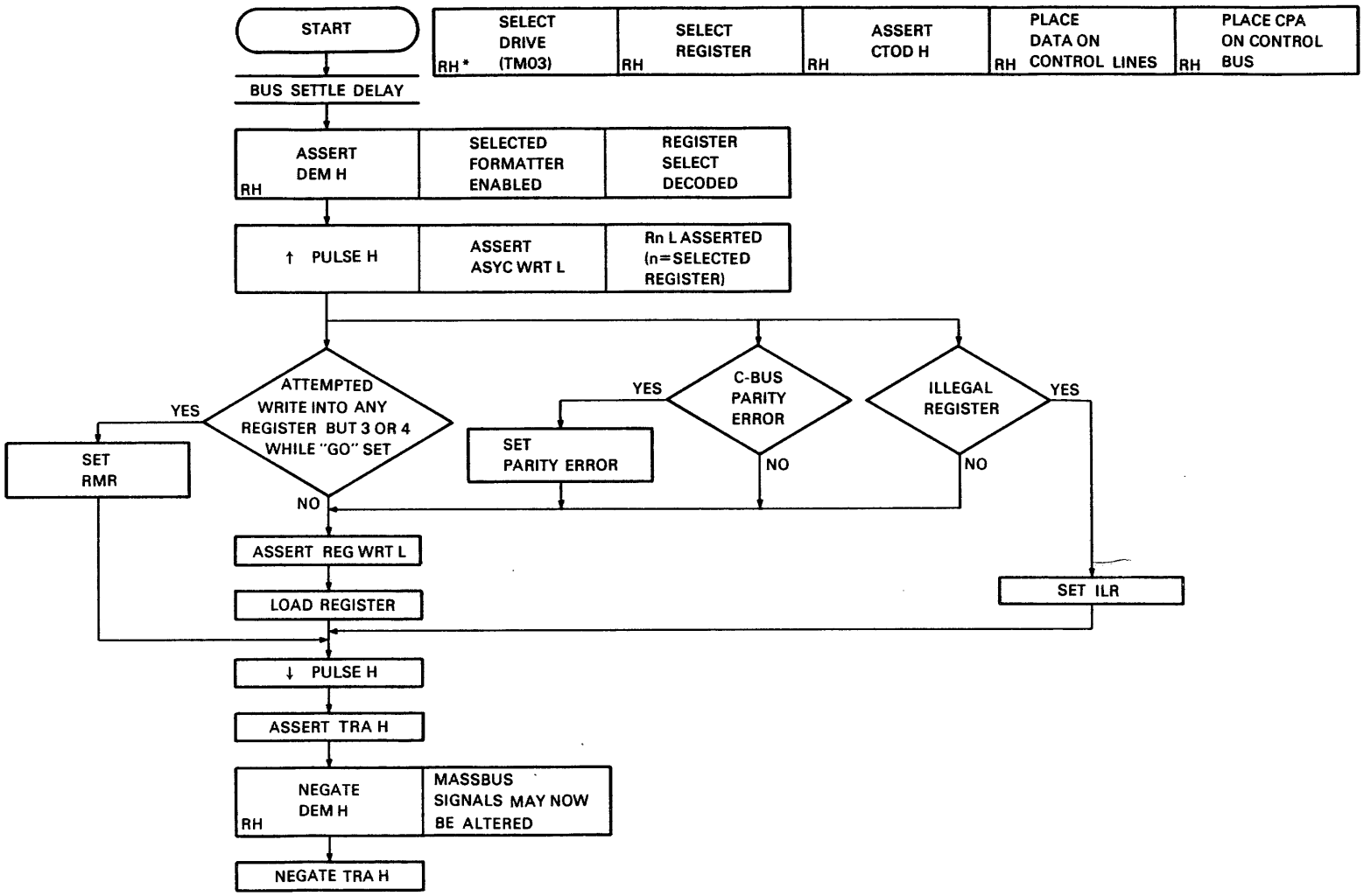
The controller now waits for these signals to settle and then asserts DEM H.

All drives daisy-chained on the Massbus examine the drive select lines (MBI2), but only the drive whose unit select jumper block configuration corresponds to the signals on the drive select lines is conditioned to respond to DEM H. All drives decode the register select lines, but only the selected drive will utilize the information on these lines.

When DEM H is received by the selected TM03, a 200 ns signal (PULSE H) is generated, which produces ASYC WRT L (also of 200 ns duration).

In the meantime:

1. The TM03 has checked for control bus parity (MBI4) and, if a parity error was detected, SET CMBPE L has been asserted.
2. The TM03 has decoded the register select lines and generated Rn L (MBI2) (where n designates the selected register). If Rn is a nonexistent register, SET ILR (set illegal register) is generated.
3. If Rn is not R3 (maintenance register) or R4 (attention summary register) and GO L is asserted (i.e., an operation other than rewind is being executed), then the TM03 generates SET RMR (set register modification refused) (MBI2).



* RH INDICATES THAT THE OPERATION IS PERFORMED BY THE MASSBUS CONTROLLER

MA-1814

Figure 4-17 Register Write Flowchart

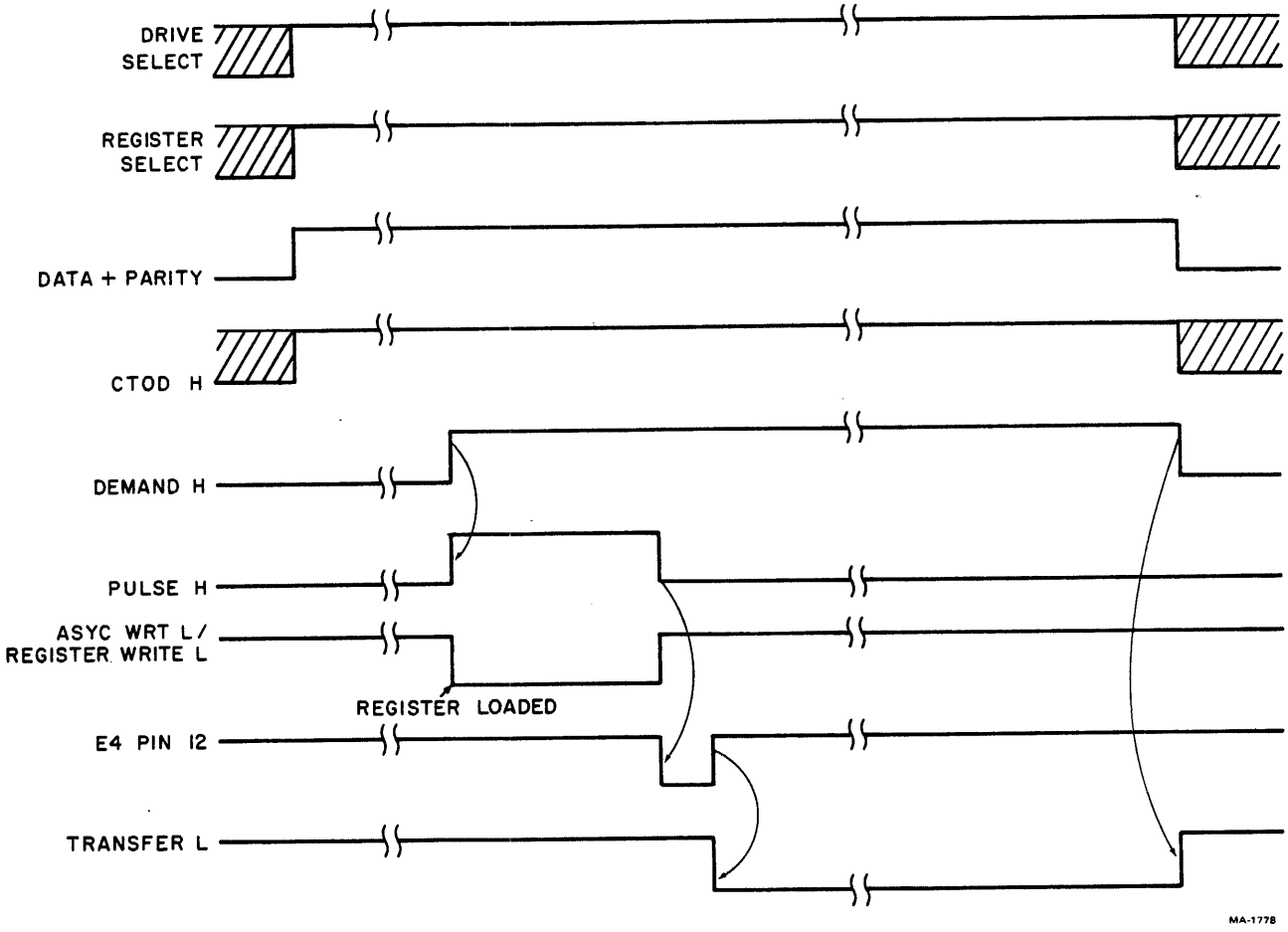


Figure 4-18 Register Write Timing Diagram

If neither SET ILR nor SET RMR has been asserted, ASYC WRT L generates REG WRT L. REG WRT L, along with Rn L, load the selected register with the data on the control lines. If SET CMBPE, SET ILR, or SET RMR were asserted, the corresponding bits in the error register are set (MBI11).

NOTE

If the control register (CS1) is being written into and there is a control Massbus parity error (CMBPE), the GO bit will not be set; therefore the command loaded into the register will not be executed.

The trailing edge of PULSE L triggers a 70 ns one-shot (MBI2). When the 70 ns one-shot times out, TRA is asserted and transmitted to the Massbus controller. This signal, when received by the Massbus controller, notifies it that the write sequence in the TM03 is over. The controller therefore negates DEM H and this in turn negates TRA (MBI1). The register transfer is over.

4.2.3.2 Register Read – The Massbus controller can read any TM03 register to determine the status of the transport or the TM03. To do so (Figures 4-19, 4-20, and 4-21), the controller simultaneously:

1. Places a 3-bit drive address code on the drive select lines
2. Places the 5-bit register select code of the desired register on the register select lines
3. Negates CTOD H.

The controller now waits for these signals to settle on the Massbus and then asserts DEM H.

Drive select recognition and register select recognition occur in the same way as for a register write (MBI2); only the selected TM03 will respond.

When DEM H is received by the selected TM03, a 200 ns signal (PULSE H) is generated. If a nonexistent register is decoded on the register select lines, SET ILR H will be generated, and, on the leading edge of PULSE H, the ILR bit of the error register will be set. If a legal register has been addressed, Rn L (as decoded from the register select lines, where n is the selected register) will multiplex the bits of the selected register to the control line latches (MR4).

The register multiplexers are located on several of the TM03 logic modules, but their outputs are "common collector wire ORed." Table 4-4 lists the modules containing the various registers and multiplexers.

Table 4-4 Register/Multiplexer Locations

Register	Bit Source	Multiplexer
00 Control	M8909-YA	M8905-YB
01 Status		M8933
02 Error	M8909-YA	M8909-YA
03 Maintenance	M8905-YB	M8905-YB
04 Attention Summary	M8909-YA	
05 Frame Count	M8909-YA	M8909-YA
06 Drive Type	Transport	M8933
07 Check Character	M8905-YB and M8901	M8905-YB
10 Serial Number	Transport	M8933
11 Tape Control	M8905-YB	M8933 and M8905-YB

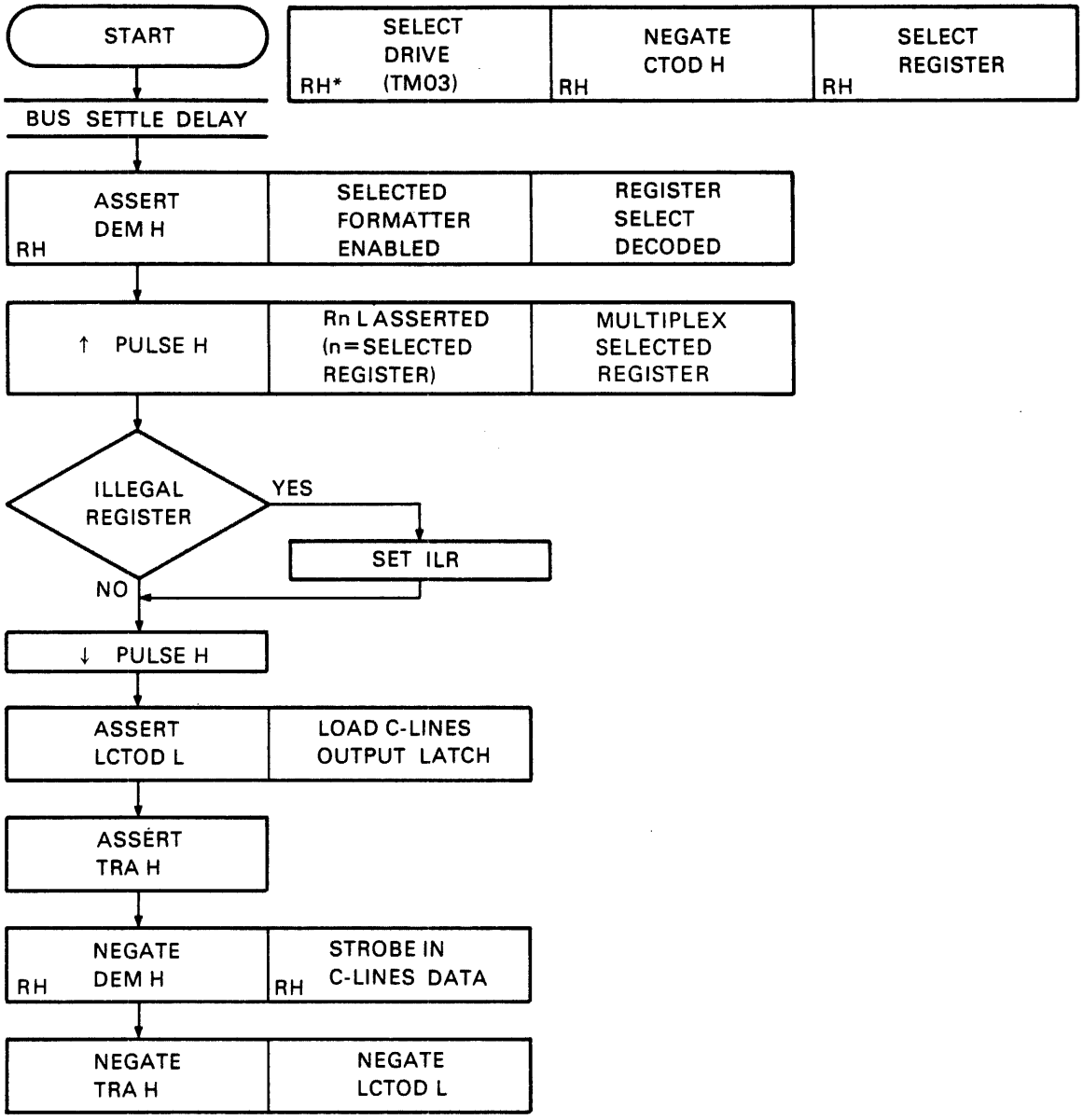


Figure 4-19 Register Read Flowchart

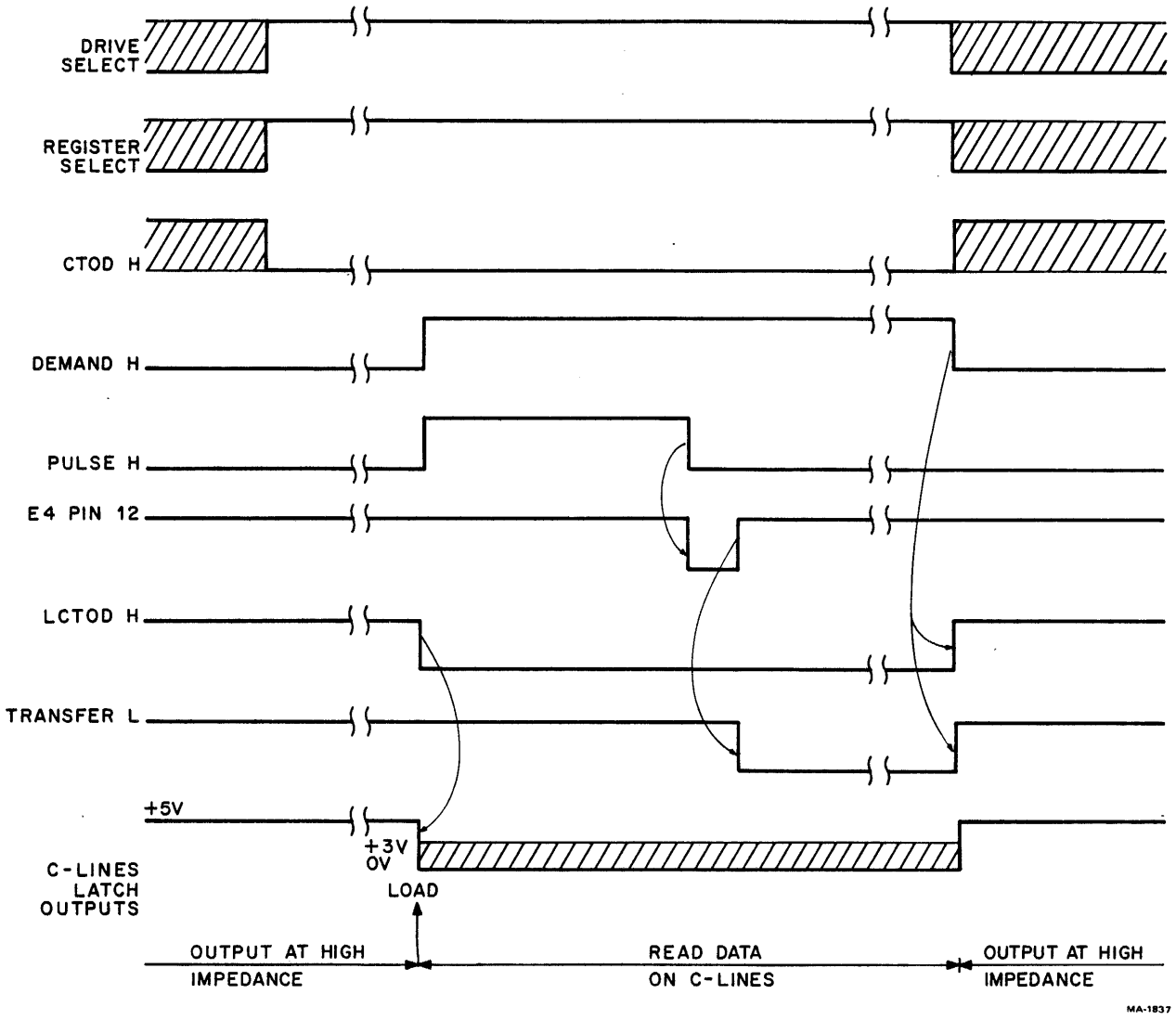


Figure 4-20 Register Read Timing Diagram

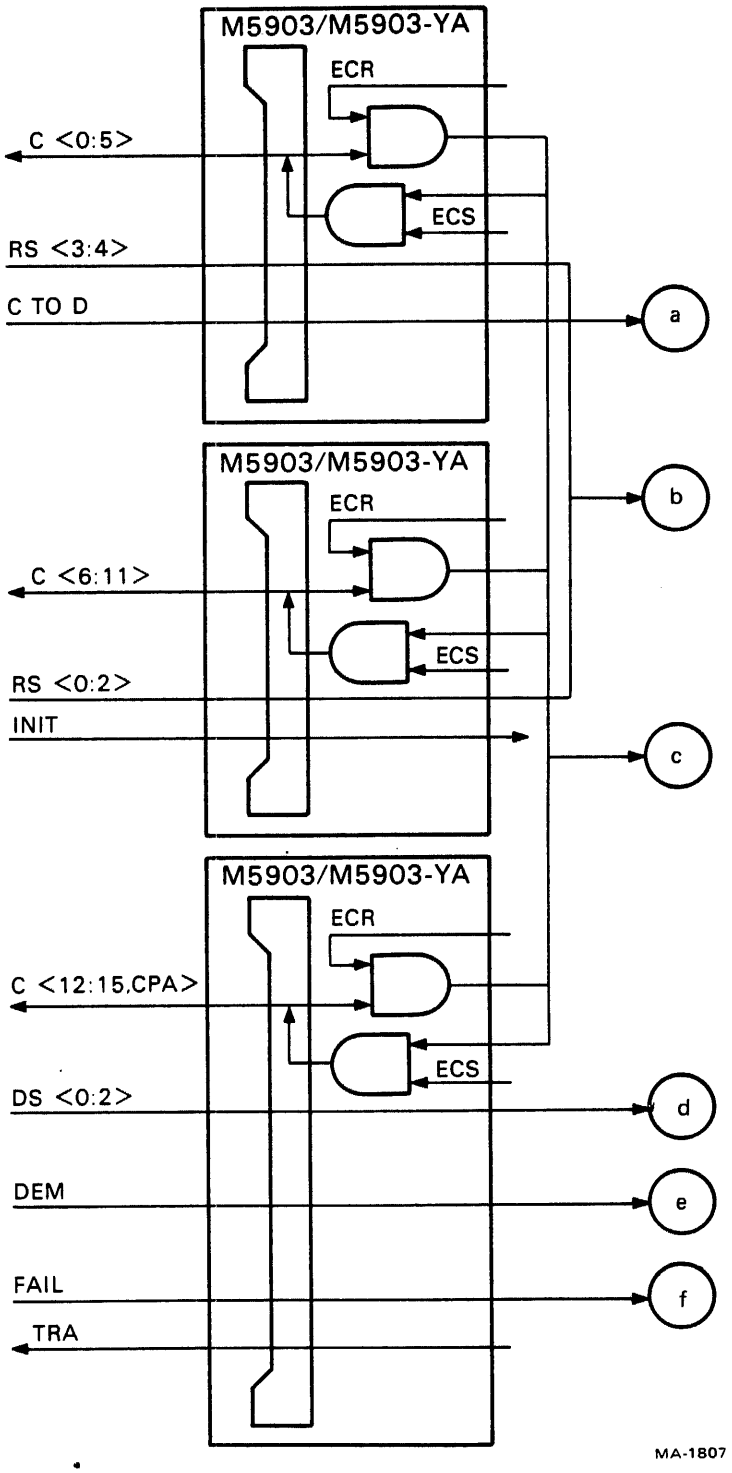


Figure 4-21 TM03 Register Read/Write (Sheet 1 of 3)

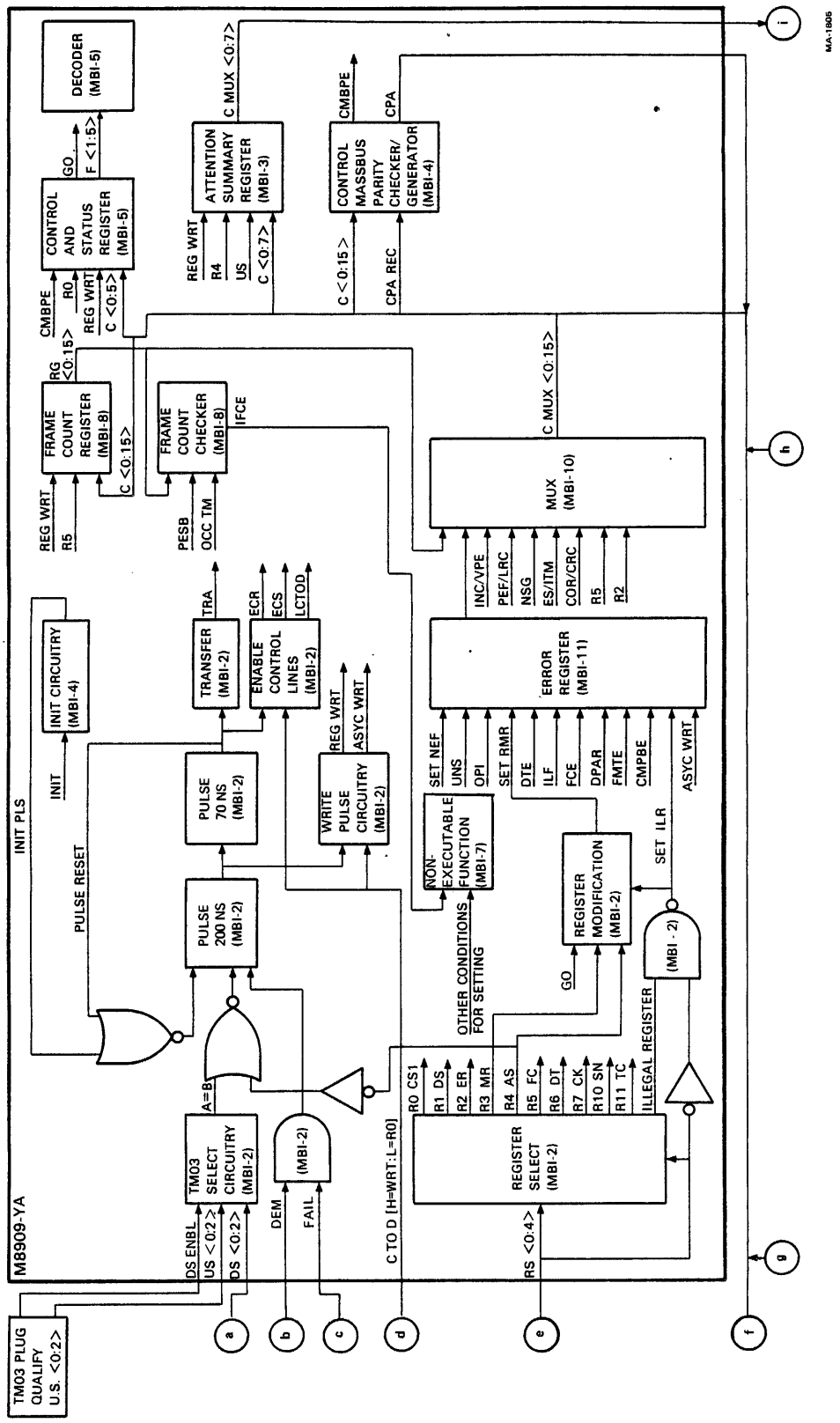


Figure 4-21 TM03 Register Read/Write (Sheet 2 of 3)

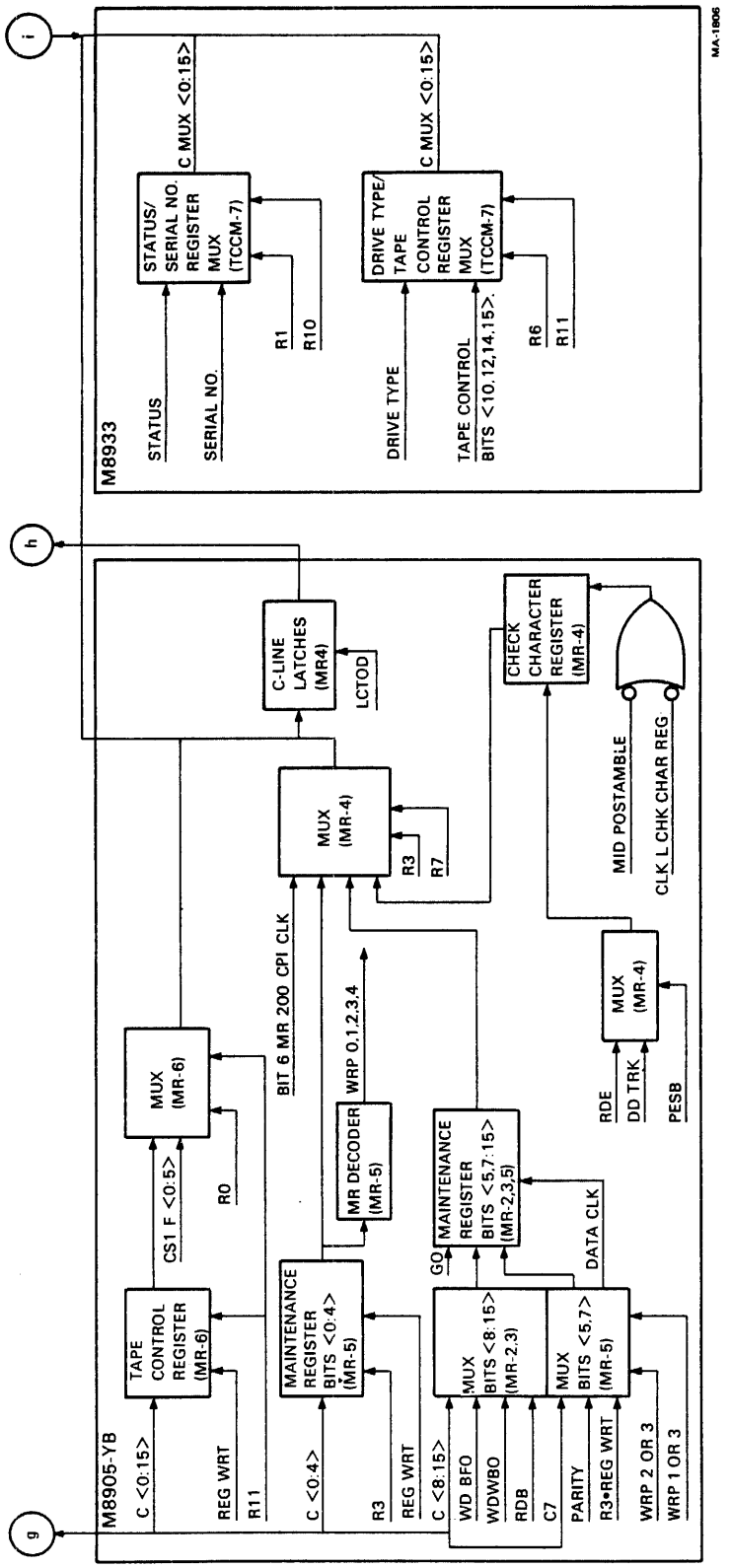


Figure 4-21 TM03 Register Read/Write (Sheet 3 of 3)

The trailing edge of PULSE L triggers a 70 ns one-shot (MBI2), which causes LCTOD L to be asserted. LCTOD loads the control line latches with the multiplexed register contents and gates the register contents onto the control lines.

When the 70 ns one-shot times out, TRA is asserted and transmitted to the Massbus controller. Upon receipt of TRA H, the controller strobes in the data on the control lines and negates DEM H. DEM H negating in turn negates TRA L in the TM03, and also negates LCTOD L. With LCTOD L negated, the control line latches produce high-level, high-impedance outputs.

4.2.3.3 Attention Summary Register (R04) – The attention summary register is shared by all TM03 formatters (and other drives) that are connected to a particular Massbus controller. Therefore, when reading or writing this register, it is not required to place any address code on the drive select lines of the Massbus. Each TM03 is enabled to respond when it decodes R4 L from the register select lines. It should be noted, however, that the DEMAND-TRANSFER "handshake" is carried on in the normal manner by the TM03.

Register 04 Read – To read the attention summary register, the Massbus controller performs its usual register read sequence; however, no particular TM03 address code need be placed on the drive select lines. When each TM03 decodes R4 L (MBI2) from the register select lines, it places its ATA (attention active) status bit on one of the control lines of the Massbus; the control line is determined by the unit select plug configuration (unit number) of the particular TM03.

A BCD decoder (MBI3 and Figure 4-22) multiplexes the ATA bit onto the proper control line. Inputs D0, D1, and D2 of the decoder are the unit select (US0–2) configuration of the TM03. If register 4 is being read and the ATA bit is asserted, input D3 is low (units 0 and 2 in Figure 4-22). The input to the BCD decoder is therefore the unit select configuration; the appropriate output is asserted low, but is later inverted by the Massbus drivers.

If the ATA bit is not asserted (unit 1 in Figure 4-22), D3 is high and the decoder decodes 8 or higher (8 + n for unit n). Since only outputs 0–7 of the decoder are used, this condition will not produce a high on the control lines.

Register 04 Write – To write the attention summary register, the Massbus controller performs the usual register write sequence. However, it need not specify a particular TM03 on the drive select lines. The DEMAND-TRANSFER handshake is carried out in the normal manner, but TM03 internal operation is slightly different.

When REG WRT L is generated, one of the control lines is multiplexed (MBI3) into the TM03. If the signal on the control line is high, it resets the ATA flip-flop; if it is low, it has no effect. The control line is selected by the unit select configuration (US0–2) of the particular TM03 input to the multiplexer.

4.2.4 Errors

This paragraph discusses the error check sequence performed by the TM03, as well as TM03 and system responses to error conditions (ATTN and EXC asserted). For a detailed discussion of the error register bits, refer to Chapter 2.

4.2.4.1 Error Check – Whenever the control register is loaded and the GO bit is set, an error check is performed. If an error condition exists, the operation specified by the function code in the control register is inhibited.

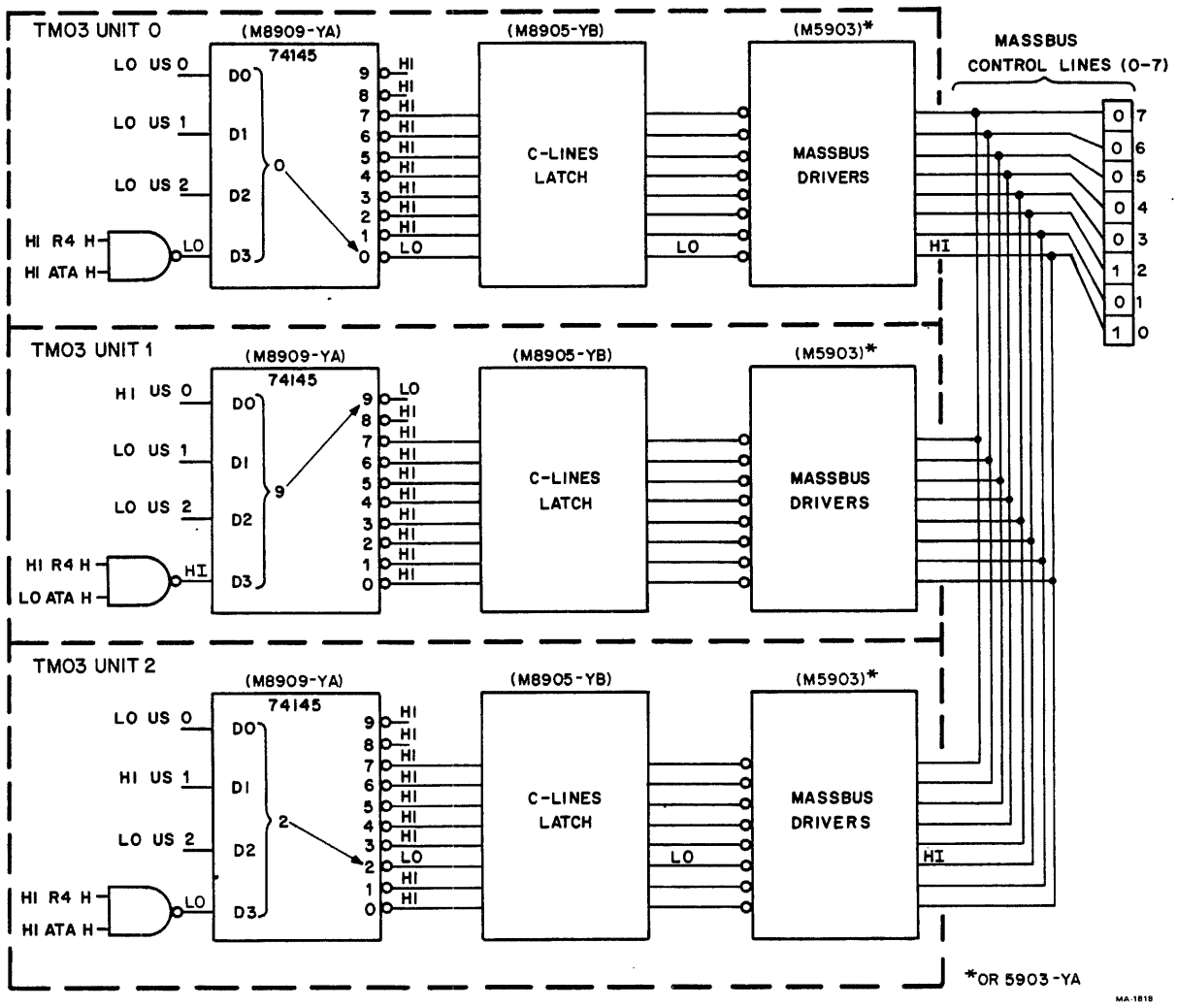


Figure 4-22 Attention Summary Register Read

If any bit in the error register is asserted, COMPER H (composite error) is asserted (MBI10). If the control register is loaded while this signal is asserted, PREV ER H (previous error) is generated and prevents the assertion of OCC (occupied) on the Massbus. This clears the control register GO bit, which in turn sets the TM03 ATA bit and asserts ATTN on the Massbus. Table 4-5 lists errors which could be detected during various operations (GO bit set). These errors will remain asserted after the operation is completed.

Table 4-5 Possible Errors During TM03/Transport Operations

Operations \ Errors	ILF	ILR	RMR	CPAR	FMT	DPAR	INC/VPE	PEF/LRC	NSG	FCE	CS/ITM	NEF	DTE	OPI	UNS	COR/CRC
Write to any register*		X	X	X												
Read from any register		X														
Load CS1 with "NO-OP"	X	X	X	X								X			X	
Load CS1 with "REWIND-OFF LINE"	X	X	X	X								X			X	
Load CS1 with "REWIND"	X	X	X	X								X			X	
Load CS1 with "DRIVE CLEAR"	X	X	X	X											X	
Load CS1 with "WRITE TAPE MARK"	X	X	X	X			X	X	X		X	X		X	X	
Load CS1 with "ERASE"	X	X	X	X							X	X			X	
Load CS1 with "SPACE FWD"	X	X	X	X						X		X		X	X	
Load CS1 with "SPACE REV"	X	X	X	X						X		X		X	X	
Load CS1 with "WRITE CHECK FWD"	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X
Load CS1 with "WRITE CHECK REV"	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X
Load CS1 with "WRITE FWD"	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Load CS1 with "READ FWD"	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X
Load CS1 with "READ REV"	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X
MASSBUS INIT															X	
Write into AS or MR register		X		X												

*Except AS or MR.

4.2.4.2 Attention (ATTN) - Attention (ATTN) is asserted on the Massbus by any drive that requires servicing. ATTN is asserted (MBI3) under the following conditions:

1. At the completion of an erase, space, or write tape mark operation
2. Upon initiation of a rewind command
3. Upon loading a 1 into the GO bit of the control register while an error condition exists
4. Upon termination of an operation during which an error occurred or SSC was asserted
5. Upon termination of any operation during which END PT was asserted.

When the Massbus controller senses that the ATTN line of the Massbus is asserted, it must read the attention summary register (R04) to determine which drive(s) require servicing. It will service each drive whose ATA bit is asserted, and will clear the ATA bit of the drive upon completion of servicing.

To service a TM03, the Massbus controller first reads the status register (R01) to determine why servicing is required. If the ERR (composite error) bit of the status register is asserted, it will read the error register (R02) to determine which error has occurred, and will then proceed accordingly. If the SSC (slave status change) bit of the status register is set, the Massbus controller should poll all the slave transports controlled by the TM03 to determine which one requires servicing and why.

4.2.4.3 Exception (EXC) - The EXC line of the Massbus is immediately asserted (MBI9) by the TM03 whenever any error occurs during a data transfer operation (OCC TM asserted).

Data transfers are normally terminated by the assertion of EBL. If during a read data operation, an error occurs that is serious enough to invalidate data, and the EAODTE bit is set, the TM03 asserts EBL (MBI9) on the Massbus. This will cause the data transfer to be terminated; however, the read data operation of the TM03 continues and terminates in the normal manner.

If during a write data operation, an error that is serious enough to invalidate data occurs, then the TM03 asserts EBL on the Massbus. It also terminates the write operation (WRITE END L asserted), stopping tape motion after erasing IRG.

The following error conditions cause the TM03 to assert EBL.

1. A data transfer operation is attempted while an error condition exists in the TM03
2. An error condition occurs while the data transfer is being initiated
3. A class B error (UNS, OPI, DTE) or an ILF error occurs while a data transfer command is being executed
4. A data error (INC/VPE, DPAR, PEF/LRC, COR/CRC) occurs during the data transfer operation, while bit 12 (EAODTE) of the tape control register is set.

4.2.5 Tape Motion - On-Line

When the slave transport is on-line, all transport operations are directed by the TM03 via the slave bus. The slave bus connects the TM03 to up to eight slave transports.

In this paragraph, transport selection and status reporting, on-line tape motion initiation, and on-line tape motion termination are discussed. Any one of several sequences can cause tape motion to terminate, depending on the type of operation being performed. Each of the termination sequences is discussed.

4.2.5.1 Transport Selection and Status Reporting – All of the tape transports in a system are wired to the same slave bus, but only one transport can be logically connected to the bus at one time, i.e., only one transport can transmit its status to the TM03 and respond to commands, and only one transport can be reading or writing data at a given time.

To select the particular tape transport to converse with the TM03, the TM03 transmits a binary code on slave bus lines SS0 (SB) L, SS1 (SB) L, and SS2 (SB) L. Each transport on the bus compares this code to its transport select number. If the selection code transmitted by the TM03 matches the transport number and the transport is on-line, the transport logically connects itself to the slave bus. All other transports remain logically disconnected and neither transmit nor respond to bus signals.

When a particular transport is logically connected to the slave bus, it transmits status information to the TM03 as follows.

7CH (SB) L	Always negated in the tape transport.
BOT (SB) L	Asserted when the tape is positioned at the load point (beginning of tape).
END PT (SB) L	Asserted when the tape is positioned at the end point.
WRL (SB) L	Asserted when the tape transport is write-locked.
RWS (SB) L	Asserted when the tape transport is performing a rewind operation
SDWN (SB) L	Asserted when the transport is settling down following an operation, i.e., asserted following the command to terminate an operation while the capstan is coming to a halt.
TUR (SB) L	Asserted when the transport is ready to receive any command, i.e., when the transport is neither performing an operation nor settling down following an operation.

4.2.5.2 Tape Motion Initiation (On-Line) – When DRV SET PLS is generated by the Massbus interface module (MBI6), the TM03 negates STOP L (TCCM3) and asserts SLAVE SET PLS L (TCCM4) and EMD L (TCCM3) on the slave bus (Figures 4-23 and 4-24). During a read or write data operation, this is a consequence of the assertion of RUN H by the Massbus controller. During nondata transfer operations that require tape motion, this is a consequence of loading the corresponding function code (GO bit set) into the control register (R00).

If a slave transport is selected, on-line, and loaded with tape (MOL H asserted), it responds to SLAVE SET PLS and the FWD, REV, and RWND command lines of the slave bus by initiating tape motion. If the WRITE command line is asserted, along with the RWND command line, the transport starts a rewind operation and is placed off-line. If WRITE is asserted but RWND is not asserted, a write data operation is started.

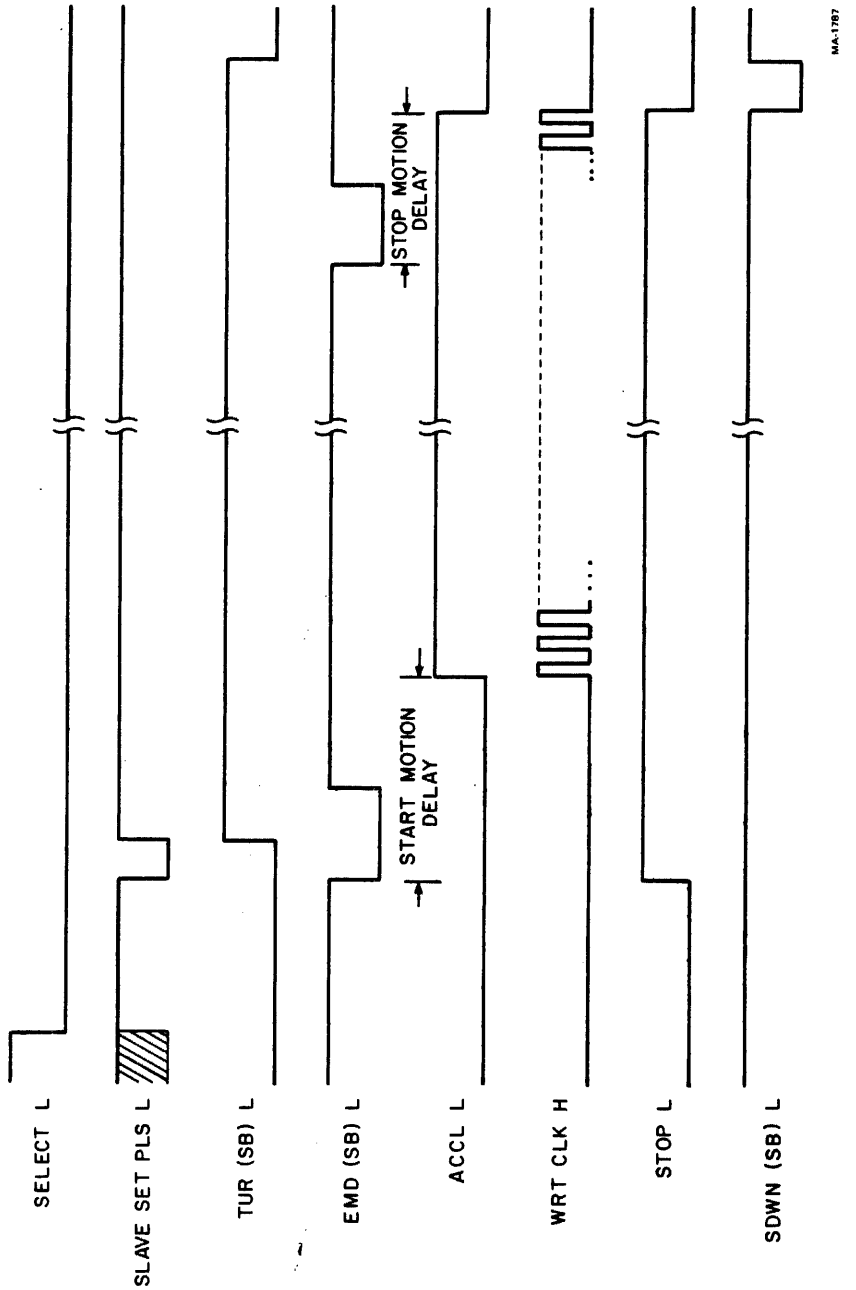


Figure 4-23 Tape Motion Timing

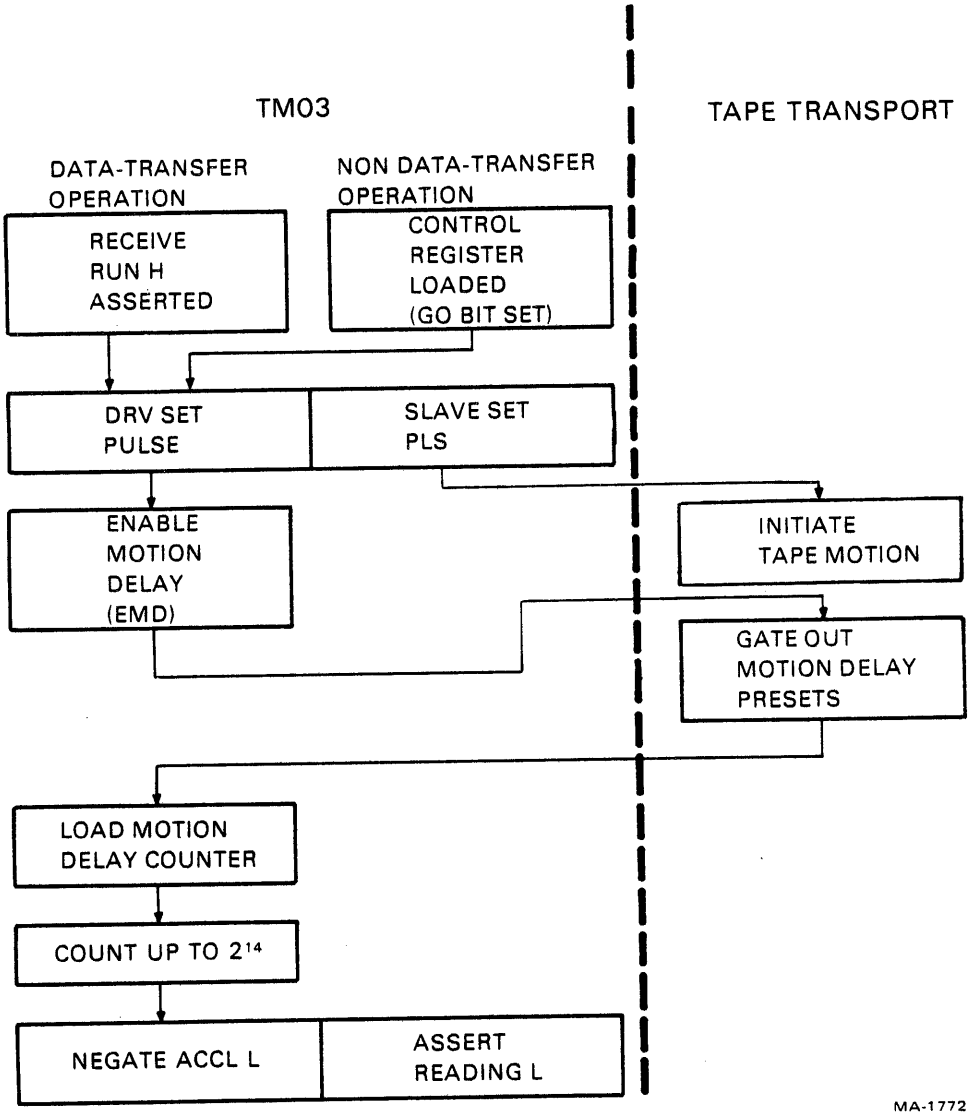


Figure 4-24 Tape Motion Initiation Flowchart

Simultaneously with motion initiation, EMD L gates the motion delay presets onto the read data lines of the slave bus and loads them into the motion delay counter in the TM03 (TCCM3). When EMD L is negated, the counter is upcounted by 800 BPI CLK until it reaches a count of 2^{14}, at which time ACCL H is negated, READING L is asserted, and further clocking of the delay counter is inhibited. The presets of the counter determine the time interval necessary to reach a count of 2^{14}, and hence the duration of the motion delay. When an erase or write tape mark operation is performed, the presets to the motion delay may be modified. The presets may vary according to the type of operation performed, the direction of tape motion, and other parameters. (See maintenance manual of particular tape transport for the motion delays generated under various conditions. The transport manuals are listed in Table 1-1.) READING L enables the read circuitry in the TM03. ACCL L negated is transmitted to the slave transport, where it enables generation of WRT CLOCK and other read and write functions.

Once forward or reverse tape motion is initiated, it continues (unless a transport mechanical or power failure occurs) until the TM03 transmits STOP L asserted to the transport.

If a rewind operation is being performed, STOP L is asserted as soon as SLAVE SET PLS is negated. However, this does not terminate tape motion as the slave transport performs the rewind operation independently. The transport notifies the TM03 that it is performing a rewind by asserting RWS L on the slave bus. When the rewind control sequence is over, motion terminates automatically. The TM03 is so notified when the transport asserts SET SSC L (slave status change) on the slave bus.

4.2.5.3 Tape Motion Termination (Read) – Refer to Figure 4-25. During a read operation, the motion termination sequence begins when the read circuitry negates RST SHDN CNTR. This occurs when the read heads encounter the IRG after reading a data record or tape mark.

When a tape mark or data record (24 preamble characters for PE, 10 data characters for NRZI) is encountered, ENBL SHDN CNTR L is asserted (TCPE5 and CNRZ4). Because WRT CLK ENBL L is not asserted during a read operation, the gap detection timer (TCCM5) will be inactive. This allows ENBL SHDN CNTR L to gate 200 BPI CLK H to the shutdown counter.

When no envelopes are detected in PE mode (ANY ENV H negated), or when no RSDO pulses are received from the slave transport in NRZI mode, RST SHDN CNTR L is negated. This allows the shutdown counter to be upcounted. If the counter reaches a count of 15, EOR PLS and EOR CLR L are produced. EOR CLR L asserts EMD L (TCCM3) and thereby initiates a stop motion delay. EMD L loads the motion delay counter with presets gated by the slave transport onto the read data lines of the slave bus, just as occurred during motion initiation (Paragraph 4.2.5.2). However, the presets will probably be different during start and stop delays.

Note that because ACCL H was negated, the two most significant bits of the motion delay counter are preset high, asserting DECL H and negating READING L. The counter is upcounted until overflow, at which time DECL H is negated and ACCL H is asserted. The leading edge of ACCL H clocks the stop flip-flop, causing STOP L asserted to be transmitted to the slave transport. STOP L causes a tape motion slow-down within the transport. As tape motion slows down, SDWN L is asserted by the slave transport and transmitted to the TM03. When tape motion stops, RUNNING H is negated, while TUR L is asserted and transmitted to the TM03.

4.2.5.4 Tape Motion Termination (Write) – Refer to Figure 4-25. Termination during a write is almost identical to that during a read. The only difference is in the gap detection timer circuit (TCCM5). During a write termination, the asserted state of WRT CLK ENBL L inhibits the gap detection timer. Thus ENBL SHDN CNTR L cannot gate clock pulses to the shutdown counter until 2.7 ms after the last character is written.

4.2.5.5 Tape Motion Termination (Erase) – Refer to Figure 4-25. Termination during an erase follows a sequence similar to that of a write. The sequence starts as soon as the start motion delay is over (READING L asserted). This causes the shutdown counter (TCCM5) to be upclocked immediately, because RST SHDN CNTR L remains unasserted. Thus the stop motion delay follows the start motion delay almost immediately, and approximately 7.62 cm (3 in) of tape is erased.

4.2.5.6 Tape Motion Termination (Space) – Refer to Figure 4-25. Termination during a space is similar to that of a read. Each time an IRG is detected, a stop motion delay is generated, and STOP L is transmitted to the slave transport. However, as soon as SDWN L asserted is received by the TM03, a DRV SET PLS is generated, which produces a start motion delay and a SLAVE SET PLS. Thus, start motion and stop motion delays are produced as each record is spaced.

Each time a record is detected, the frame count register is incremented. When the frame count register overflows, or when a tape mark is detected, further DRV SET PLS pulses are inhibited and tape motion ceases.

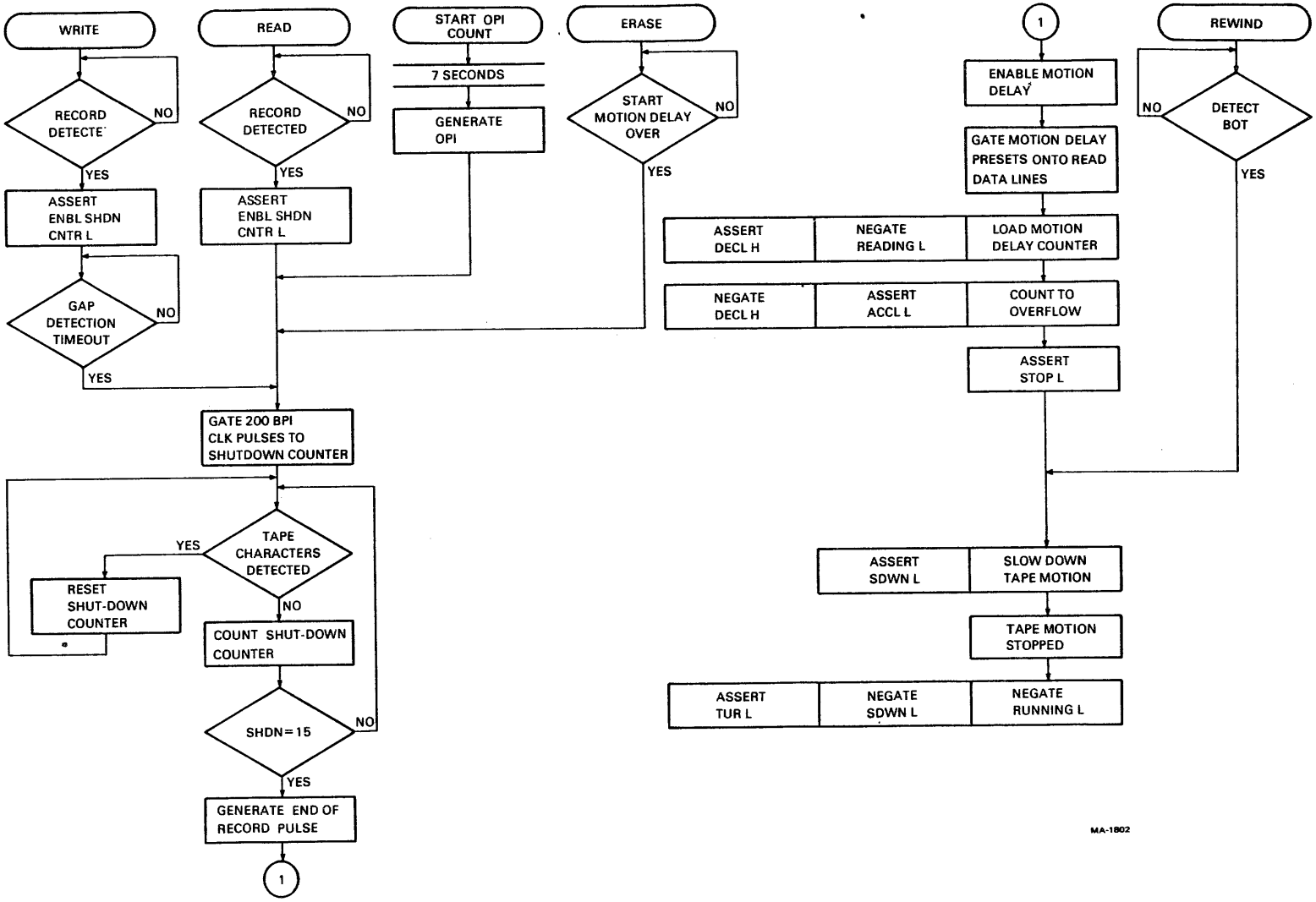


Figure 4-25 Tape Motion Termination Flowchart

4.2.5.7 Tape Motion Termination (Rewind) – Refer to Figure 4-25. When the transport starts a rewind operation, it asserts RWS L on the slave bus and performs the rewind operation in an independent manner. When tape motion ceases, RWS L is negated and SET SSC L is asserted on the slave bus.

4.2.5.8 Tape Motion Termination – Operation Incomplete (OPI) – Refer to Figure 4-25. The OPI bit of the error register is set when the end of a record is not detected within 7 seconds of the initiation of a read, write, or space operation.* If OPI H is asserted, 200 BPI CLK H is gated to the shutdown counter. The shutdown sequence begins when RST SHDN CNTR L is negated. Thus, if a record has not been detected, shutdown begins immediately. If a record is being detected, the shutdown sequence begins at the end of the record.

4.2.6 Density Select/Tape Speed Select

4.2.6.1 Density Select

NOTE

The functional block diagram of Figure 4-28 uses logical AND and OR symbols. It does not necessarily follow that a corresponding gate exists on the TM03 logic prints. The assertion of inputs A and B causing the assertion of output C may be represented on a block diagram by a single AND gate, yet the engineering drawing may show that several circuit stages are involved in the ANDing operation.

The signal names used on the functional block diagram are the names used on the engineering circuit schematics (CS prints). Where other signal names or notes are used, they are enclosed in parentheses.

Density Select for a Read Command – Figures 4-26, 4-27, and 4-28 illustrate the density selection process in the TM03. When the transport is at BOT, the tape is positioned as shown in Figure 4-26. The read/write head assembly is positioned over the tape leader where noise may exist. When the transport is commanded to read the tape, DRV SET PLS is asserted, causing SLAVE SET PLS to be asserted to the slave transport. SLAVE SET PLS initiates tape motion in the transport; however, ACCL is asserted on the slave bus and inhibits the transport read logic.

The assertion of DRV SET PLS sets a PE flip-flop on the control and write driver module (M8937) which, via an enabled read gate, causes 1600 BPI to be asserted. This in turn asserts DEN2 (SB) to the slave transport, placing it in the PE mode of operation. In addition, DRV SET PLS causes a 4.3 cm (1.7 in) counter to be enabled via a counter enable flip-flop. After the preset startup delay has timed out, the tape has advanced to where the ID burst (if there is one) is over the read heads. At this point, ACCL is negated on the slave bus, enabling the transport read logic. Also READING becomes true and allows clocking of the 4.3 cm (1.7 in) counter by the 200 bits/in signal. The 4.3 cm (1.7 in) counter reaches a count of 10 after an additional 4.3 cm (1.7 in) of tape has been read. [The frequency of 200 bits/in is proportional to tape speed. Therefore 4.3 cm (1.7 in) of tape will be traveled when 10 COUNT asserts, regardless of tape speed.] While the 4.3 cm (1.7 in) of tape is being traveled, the TM03/transport read logic is looking for the ID burst. If a burst is found, IDB will assert (Paragraph 4.2.7.6). The 10 COUNT output from the counter clocks the PE flip-flop, which will remain set. If no identification burst is found, IDB will be false and the PE flip-flop will reset. If the PE flip-flop resets, 1600 BPI and DEN2 (SB) negate and the transport goes into the NRZI mode for the first record. When the 4.3 cm (1.7 in) counter reaches its maximum count, the CO (carry out) output is asserted, thereby disabling the counter via the counter enable flip-flop, until the flip-flop is set again by another DRV SET PLS while at BOT.

*Thus from 8 to 22.3 meters (26 ft, 3 in to 73 ft) of tape will move past the read/write heads, depending on transport speed, during an OPI time-out.

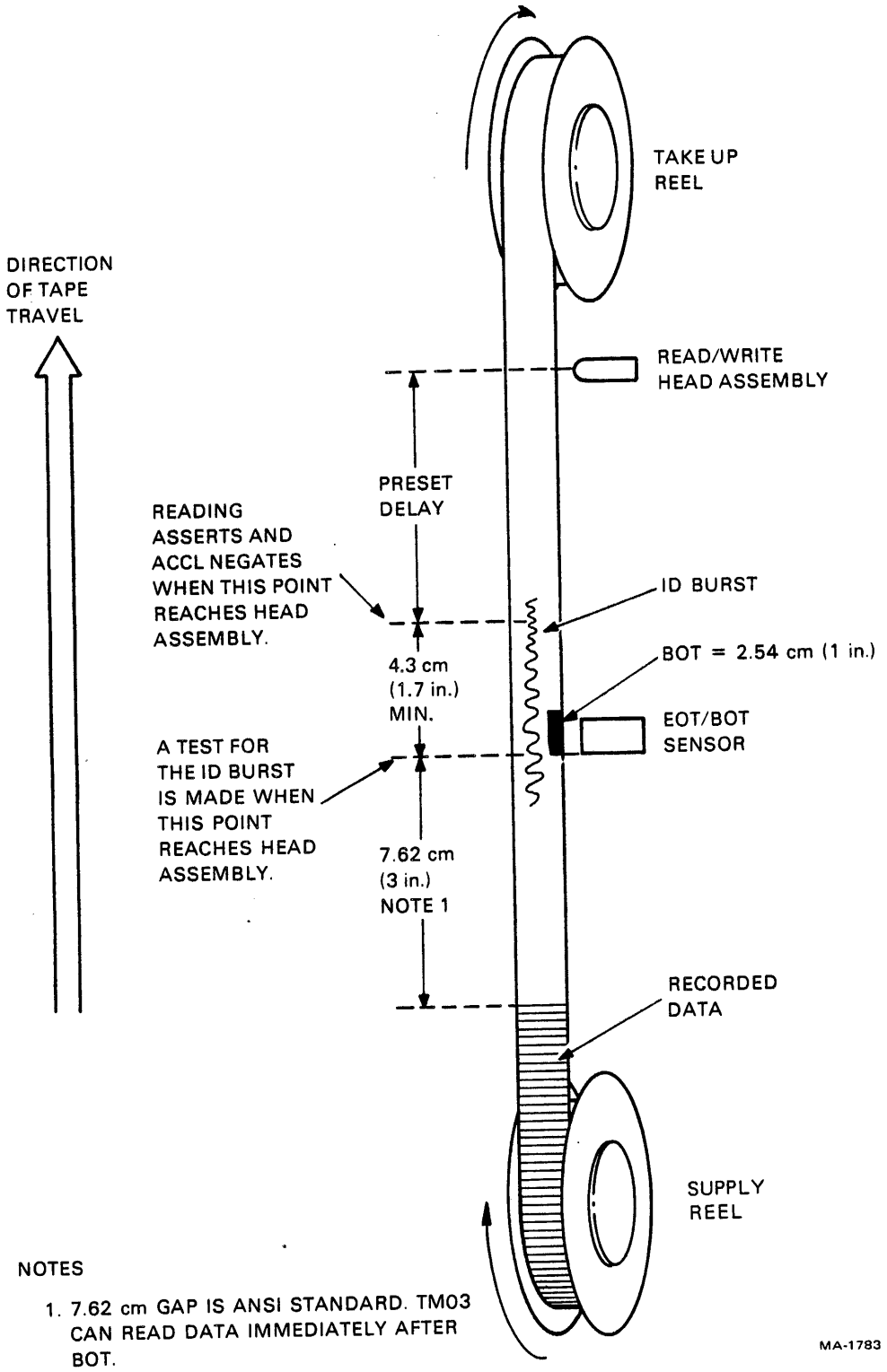


Figure 4-26 Magnetic Tape Positioned at BOT

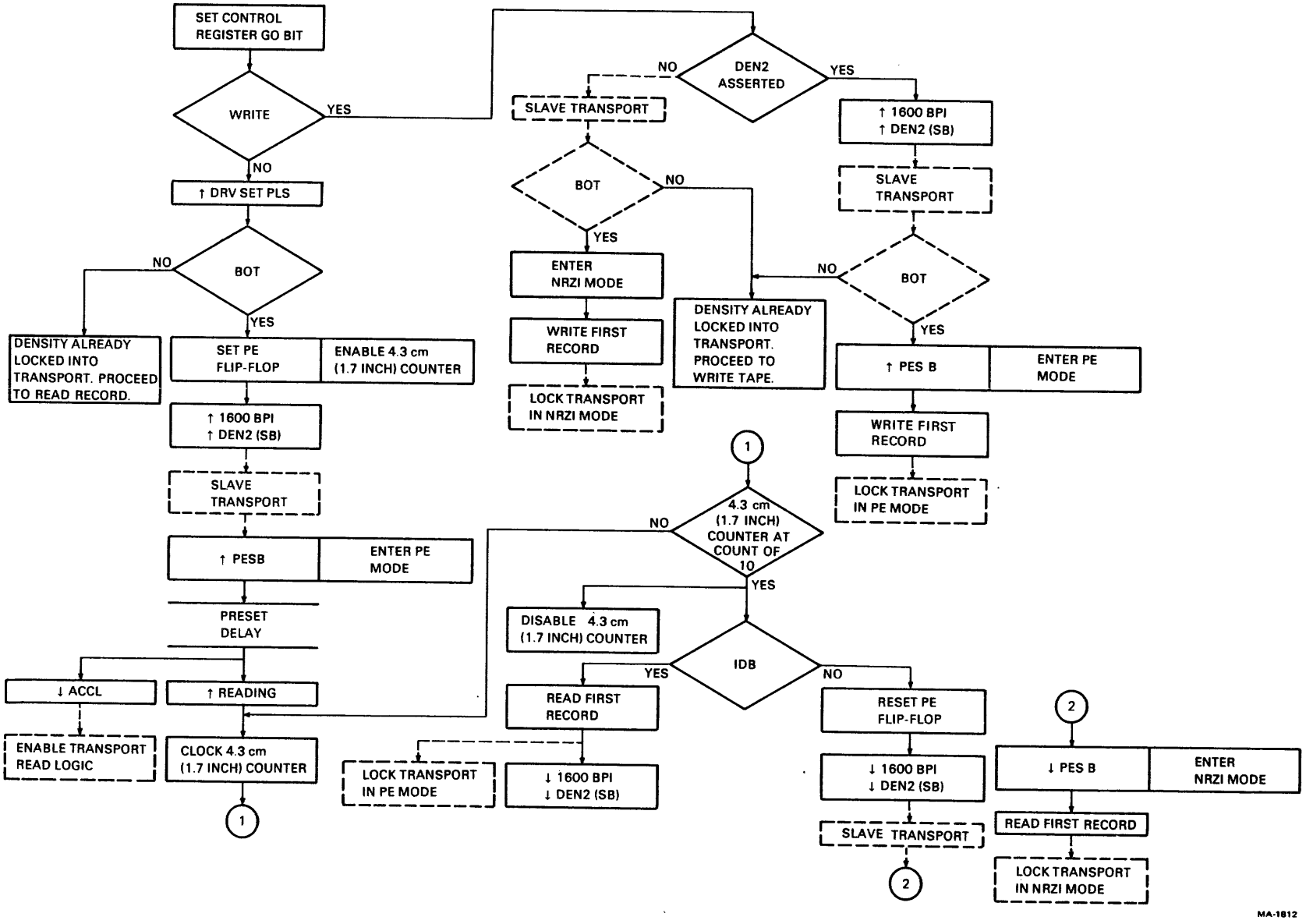


Figure 4-27 Density Select Flow Diagram

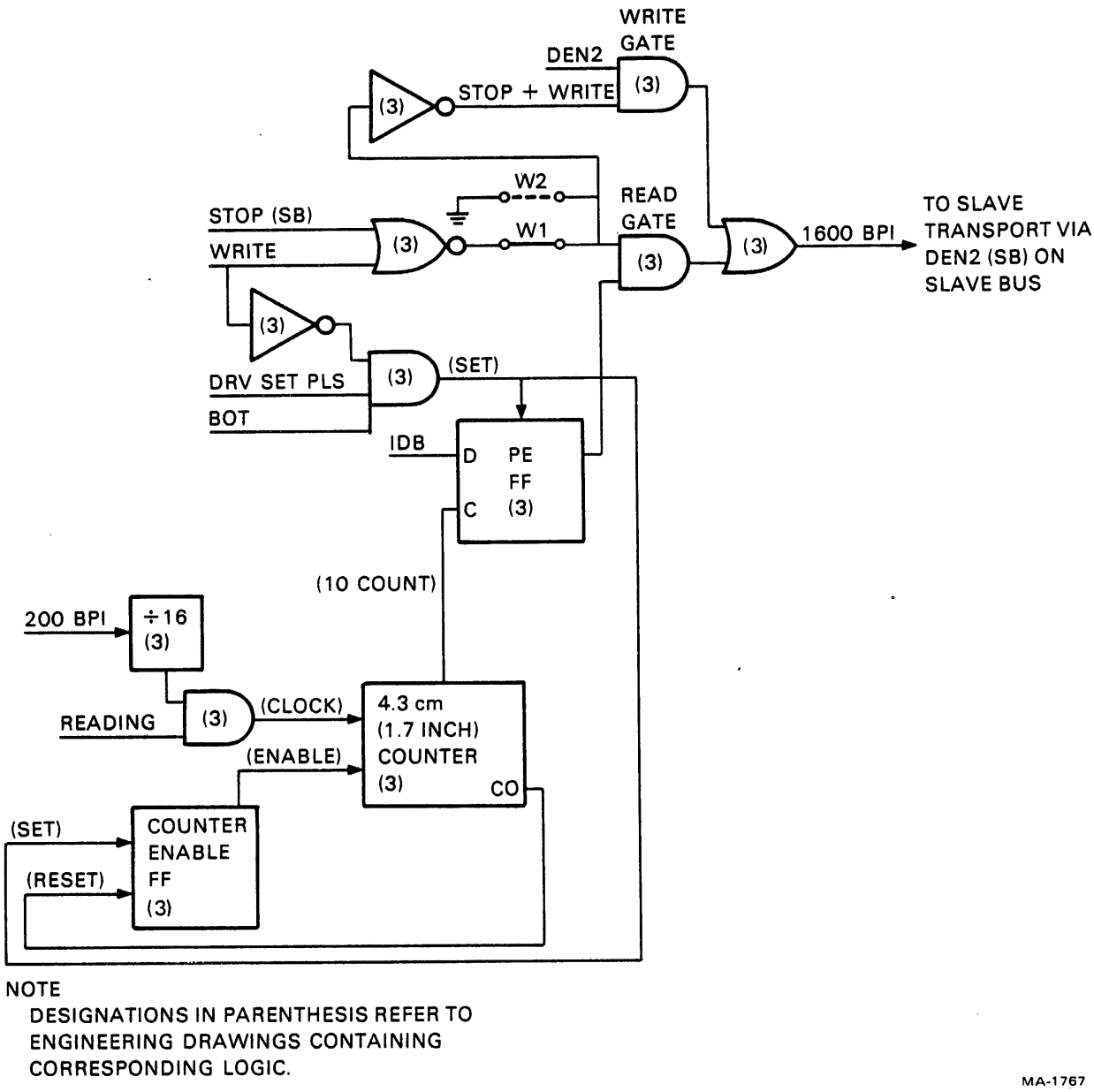


Figure 4-28 Density Select Block Diagram

To summarize the preceding: after the preset delay has expired, the TM03/transport searches for an ID burst for 4.3 cm (1.7 in) of tape. At the end of the 4.3 cm (1.7 in), a check is made for the presence of IDB. If IDB is found true, the slave transport remains in the PE mode and reads the first record. If no burst is found, the slave changes to the NRZI mode and reads the first record.

Figure 4-26 shows a 7.62 cm (3 inch) gap between BOT and the recorded data. The gap is an ANSI standard and not a result of TM03 or transport limitations. The TM03 is capable of reading data as soon as the 4.3 cm (1.7 in) segment has passed the read heads (right after BOT).

After the first record has been read, the transport is latched into the mode used to read the first record. The transport will read only in this mode for the rest of the tape. This is true even though the transport is deselected and then selected again at a later time. When the transport is commanded to read from BOT, a check is again made for an ID burst and the process is repeated to automatically select the tape density (mode).

Density Select for a Write Command – When a write command is asserted by the TM03, the read gate is inhibited and the write gate is enabled. The state of the DEN2 line determines the mode of operation. If DEN2 is true, 1600 BPI is asserted, thereby asserting DEN2 (SB) to the slave transport and the first record is written in the PE mode. If DEN2 is false, 1600 BPI and DEN2 (SB) are false and the first record is written in the NRZI mode. As in the case for a read operation, after the first record has been written, the transport is latched into the mode used to write the first record. The transport will write only in this mode for the rest of the tape. This is true even though the transport is de-selected and then selected again later. When the transport is commanded to write from BOT, the DEN2 line again becomes effective in selecting the recording mode for the data.

Note in Figure 4-28 that STOP (SB) is ORed with WRITE to enable the read or write gate. STOP (SB) is true until SLAVE SET PLS is issued to the transport to initiate tape motion (Figure 4-29). During this time, the read gate is inhibited and the write gate is enabled (DEN2 controls the state of 1600 BPI). When SLAVE SET PLS asserts, STOP negates, thus allowing the state of WRITE to determine whether the read gate or the write gate is enabled.

The purpose of forcing the write gate into the enabled state until SLAVE SET PLS occurs is as follows. When a write operation is commanded, the TM03 checks that the transport is in the correct mode by testing the PES line on the slave bus. If the transport mode does not agree with that commanded by the TM03, a non-executable function error is generated. The check for transport density mode is made when GO asserts. As seen in Figure 4-29, the state of DEN2 is established prior to the assertion of GO; however, WRITE asserts simultaneously with GO and would not gate DEN2 (SB) to the transport to establish PES status soon enough to prevent an NEF error. By using STOP (SB) to initially enable the write gate, DEN2 (SB) can be received by the transport and the transport status (PES) returned to the TM03 by the time GO asserts.

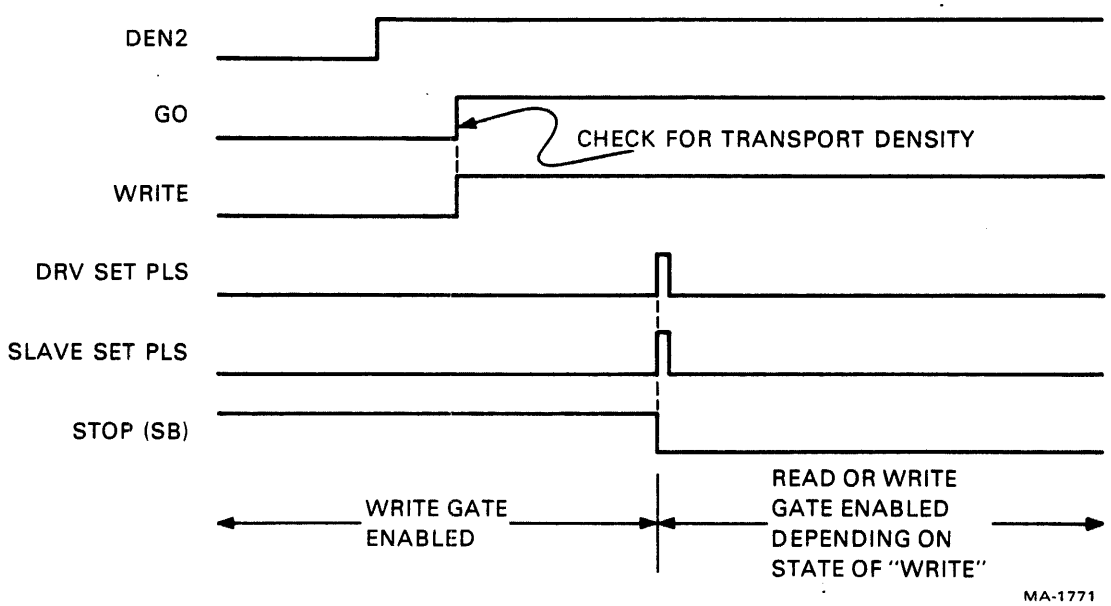


Figure 4-29 Density Select Timing

The operation of the auto density select feature functions as just described with jumper W1 installed and W2 removed. To disable the auto density feature, remove jumper W1 and install W2.* This will inhibit the read gate and enable the write gate, thereby placing the DEN2 (SB) line on the slave bus constantly under the control of DEN2.

4.2.6.2 Tape Speed Select – Figure 4-30 is a block diagram of the tape speed selection process. The 200 bits/in clock is passed through a frequency divider and output as TAPE SPEED CLK. The drive type code (DT1, DT2) from the slave transport establishes the count-down factor for the frequency divider. The frequency of TAPE SPEED CLK for a 114.3 cm (45 in/s) transport is the 200 bits/in rate of 9 kHz (no frequency division). The frequency of TAPE SPEED CLK for a 190.5 cm/s (75 in/s) transport and a 317.5 cm/s (125 in/s) transport is the 190.5 cm/s (75 in/s), 200 bits/in rate divided by 2, and the 317.5 cm/s (125 in/s), 200 bits/in rate divided by 4, respectively (Table 4-3). TAPE SPEED CLK is used for display monitoring during maintenance mode read operations.

The transport drive type code is also applied to a tape speed decoder which asserts 45 IPS L, 75 IPS L, or 125 IPS L, depending on the speed of the selected transport. The outputs from the tape speed decoder are applied to the data sync module inserted into slot CDEF01. All three data sync modules are identical, with each having three pairs of jumper terminals, one pair of which will have jumpers installed according to the speed of the module. The data sync module in slot CDEF03 outputs a SET NEF H signal to M8909, which, when asserted, will set the non-executable function (NEF) bit in the error register. To hold the SET NEF H signal negated (low), it is necessary that:

1. All three data sync modules be the same tape speed, and

2. The asserted (low) output of the tape speed decoder agree with the tape speed of the data sync modules.

Figure 4-30 shows jumpers installed for 114.3 cm/s (45 in/s) modules (M8901-YB).† If the tape speed decoder decodes a 114.3 cm/s (45 in/s) tape speed from the DT inputs, 45 IPS L is asserted and coupled to the M8909 Massbus interface module, pulling down the SET NEF H signal line, and thereby negating SET NEF H. If the decoder decodes 75 IPS L or 125 IPS L from the DT inputs, or if all three data sync modules are not M8901-YBs, SET NEF H asserts and an error condition prevails.

4.2.7 Read (PE)

This paragraph discusses the operation of the TM03 read circuitry when operating in PE mode. The PE read data path (reference Figure 4-4) is covered from the slave bus to the inputs of the bit fiddler. (Bit fiddler read operation is described in the latter paragraphs of this chapter.) The read data signals are received from the slave bus by the receiver terminator module (M8908-YA). The signals are then transmitted to the TCCM module in the TM03 where they are multiplexed to the three data sync modules (M8901).

*A jumper change is also required in the slave transport.

†M8901-YC = 190.5 cm/s (75 in/s) module.
M8901-YD = 317.5 cm/s (125 in/s) module.

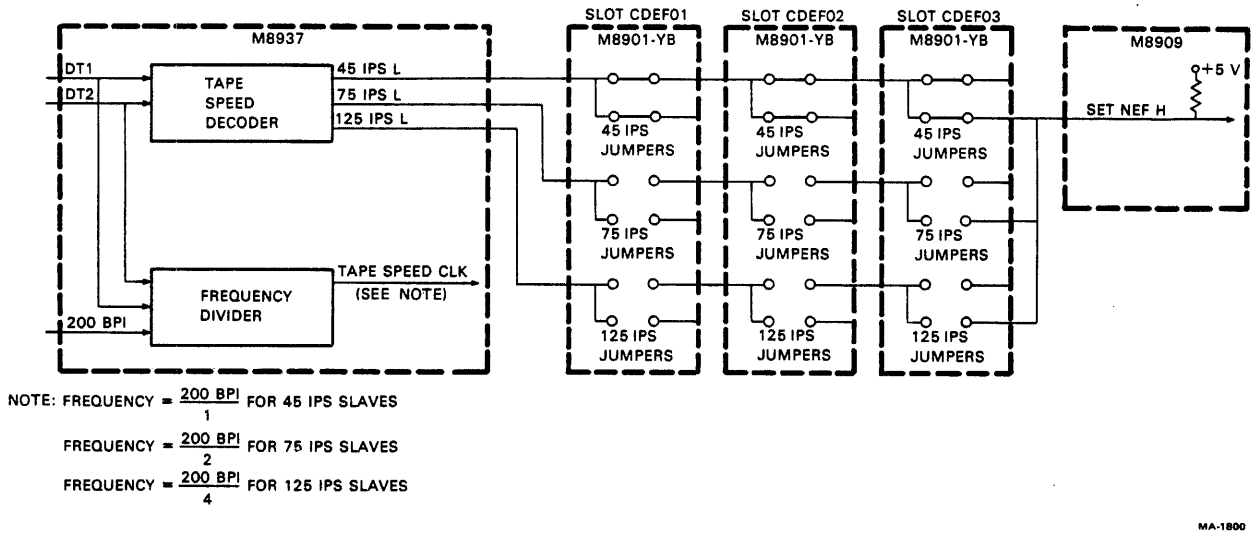


Figure 4-30 Tape Speed Selection Block Diagram

4.2.7.1 Data Sync – The data sync module (M8901)* contains three identical sections, each of which processes a single track of read data (Figure 4-31). Each of these sections contains a data discriminator, a phase-locked clock, a deskew buffer, error detection circuitry, and error correction circuitry (Figure 4-32). To process nine tracks of data, three data sync modules are required.

NOTE

Operation of all sections of the M8901 data sync module is identical. Therefore, only one section is discussed unless otherwise specified.

Phase-Locked Clock – Conversion of phase-encoded data into binary data requires generation of a data window for each track, in sync with the data transitions in the track. The direction of the data transition within the data window determines whether a 1 or a 0 bit is detected.

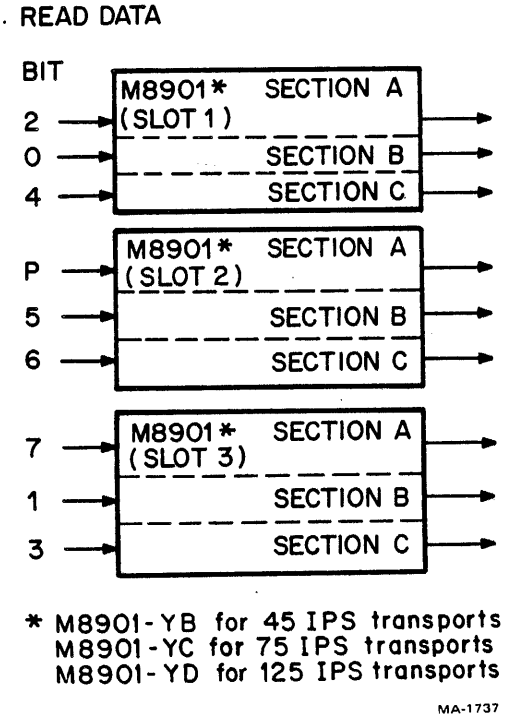


Figure 4-31 Data Sync Channels

*Throughout the following discussions the data sync module is given as M8901. The specific module used depends on the tape speed of the slave transport, i.e.,
M8901-YB for 114.3 cm/s (45 in/s) slaves
M8901-YC for 190.5 cm/s (75 in/s) slaves
M8901-YD for 317.5 cm/s (125 in/s) slaves.

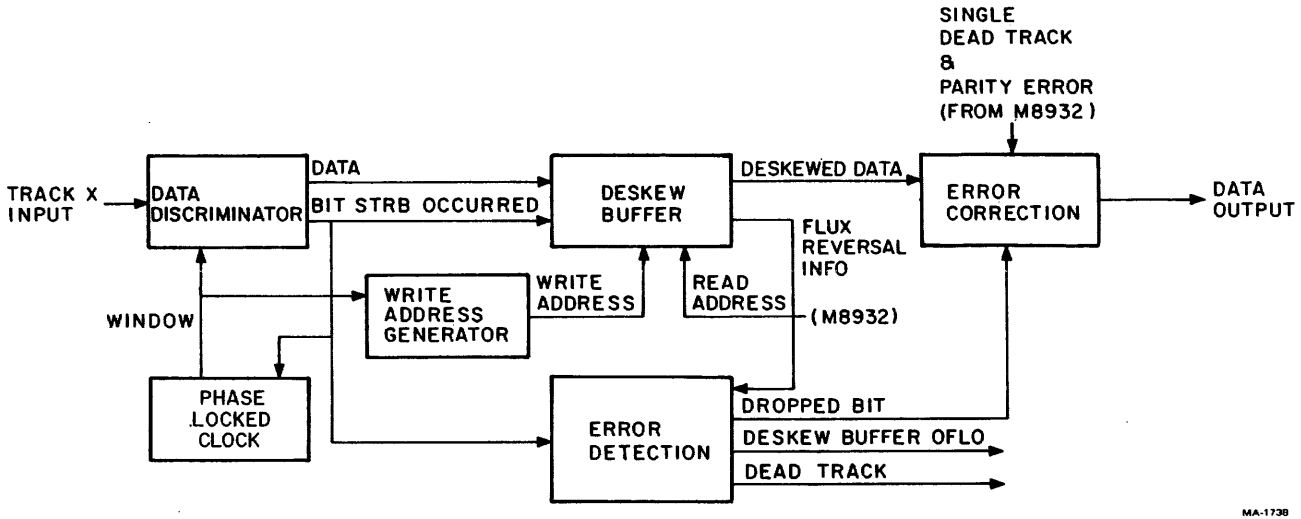


Figure 4-32 One Section of the Data Sync Module

The phase-locked clock (DS3) operates to generate the data window and to keep it in sync with the incoming data stream. The heart of the phase-locked clock is a voltage-controlled oscillator (VCO) and a phase detector. The phase detector senses the phase relationship between incoming data transitions (BIT STRB) and the VCO output signal divided down to the data frequency. If the frequency of data transitions increases (decreases), BIT STRB begins to lead (lag) TP3. This increases (decreases) the VCO output frequency and brings the two signals back in phase. Thus, the frequency of TP3 becomes the same as the frequency of BIT STRB. The data window (WINDOW) is generated 90 degrees out of phase with TP3 (DS3 and Figure 4-33).

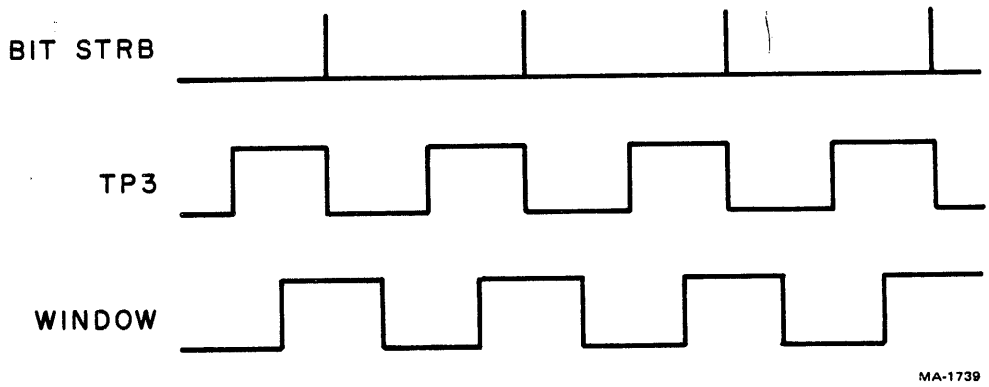


Figure 4-33 Data Window Generation

Data Discriminator – The data discriminator converts the phase-encoded data on its track into binary form: 1 = high, 0 = low. To do so, the data window must first be synchronized to the frequency of the incoming data. It is for purposes of synchronization that the preamble is used.

To understand the operation of the data discriminator, it should be noted that the data discriminator operates in three modes.

1. During the start of motion delay, ACCL is asserted on the slave bus, inhibiting the read amplifiers in the slave transport. During this time, the ID pattern cannot be detected (Paragraph 4.2.7.6).

2. When the motion delay times out, ANY TRANS is negated. During this condition, preamble 0s may be detected (Paragraph 4.2.7.2).

3. When 24 preamble 0s (20 0s for a write operation) are detected, RECORD ACTIVE and ANY TRANS are asserted. During this condition, the preamble 1s character and data are detected (Paragraph 4.2.7.3).

Deskew Buffer – The deskew buffer stores the binary data detected by the data discriminator until a whole tape character becomes available (output from all nine channels). Because eight bits of data can be stored for each channel, a skew of up to seven tape characters can be accommodated.

The deskew buffer consists of a 2 by 8 random access register. The register buffers data (RD BUFFER I) and flux reversal information (BIT STRB OCCURRED) for a single track. The register is loaded as data bits become available. The output of the register depends on its RD ADDR input (common to all channels that make up the nine tracks), and is read when a whole tape character becomes available. The RD ADDR is then incremented, and the read circuitry waits for the next tape character to become available. Deskew buffer operation is described in more detail in Paragraph 4.2.7.3.

Error Detection – The error detection circuitry senses when a data transition fails to occur. Error detection is described in more detail in Paragraph 4.2.7.3.

Error Correction – The error correction circuitry performs on-the-fly error correction. Error correction is described in more detail in Paragraph 4.2.7.3.

4.2.7.2 Preamble Detection – Because all sections of the data sync modules operate in the same manner, this discussion describes the operation of only one section: M8901, section A (DS2 and DS3). Refer to Figures 4-34 and 4-35.

The preamble 0s (A RDA H) are input to an XOR gate and an OR gate. The XOR gate inverts A RDA H if tape motion is in the forward direction (REV L negated). The output of the OR gate is of proper polarity for both forward and reverse read operations. Another XOR gate, together with an inverter and their associated circuitry, function to produce a positive pulse (BIT STRB H) each time the output of the OR gate transitions. However, because ANY TRANS is negated, and the OR gate output and BIT STRB H are "common collectored," BIT STRB H pulses are produced only on negative-going transitions. (The negative-going transitions correspond to the data transitions of preamble 0s.)

Each time BIT STRB is detected, it is fed into a one-shot which generates an envelope signal (ENV H). The one-shot time-out is about 1-1/2 character widths. Therefore, BIT STRB pulses keep the one-shot in the set state and ENV H stays asserted for the entire record.

When ENV H is detected on three tracks (TCPE4), a clear input is removed from the character counter, allowing it to be upcounted by DATA HALF H. Because DATA HALF occurs at the PE data rate, the outputs of the character counter represent the number of preamble 0s read. When the character counter reaches a count of eight (CT 3 H asserted), the preamble flip-flop is set (TCPE5). When the character counter reaches a count of 24 (CT 3 H and CT 4 H asserted), the record active flip-flop is set. With RECORD ACTIVE asserted, ANY TRANS L is asserted, and the data discriminator operates in its third mode. By this time, the phase-locked clock is synchronized to produce WINDOW H in sync with the data being read.

As preamble 0s continue, WINDOW H is always asserted at the time BIT STRB transitions low. This transition produces a BIT STRB H pulse which clocks the read buffer. But because BIT STRB is already low, the buffer remains reset.

4.2.7.3 Data Detection – When the preamble 1s character appears (Figure 4-34), BIT STRB H is produced at the positive transition of the OR gate output (DS2), thereby setting the read buffer flip-flop. Because WINDOW H has been synchronized to the PE data transition time, BIT STRB H occurs only during the data transition time, and will set or clear the read buffer depending on the direction of transition. Therefore, the binary output of the read buffer is a decode of the RDA phase-encoded data.

Deskew Buffer – Whenever WINDOW H is negated, the deskew buffer (DS3) is loaded with the contents of the read buffer and bit strobe occurred flip-flops. However, during the preamble, only location 000 is loaded each time. When the preamble 1 bit is detected, ONE DETECTED (1) H is asserted. ONE DETECTED (1) H enables the write address generator to increment the deskew buffer write address. Thus, the preamble 1s bit is loaded into address 000. The next bit, i.e., the first data bit, is also loaded into address 000 (Figure 4-36). The address is now incremented on each leading edge of WINDOW H, so that the second data bit is loaded into 001, the third into 010, etc. After the eighth data bit, the write address becomes 000 again, and the cycle continues.

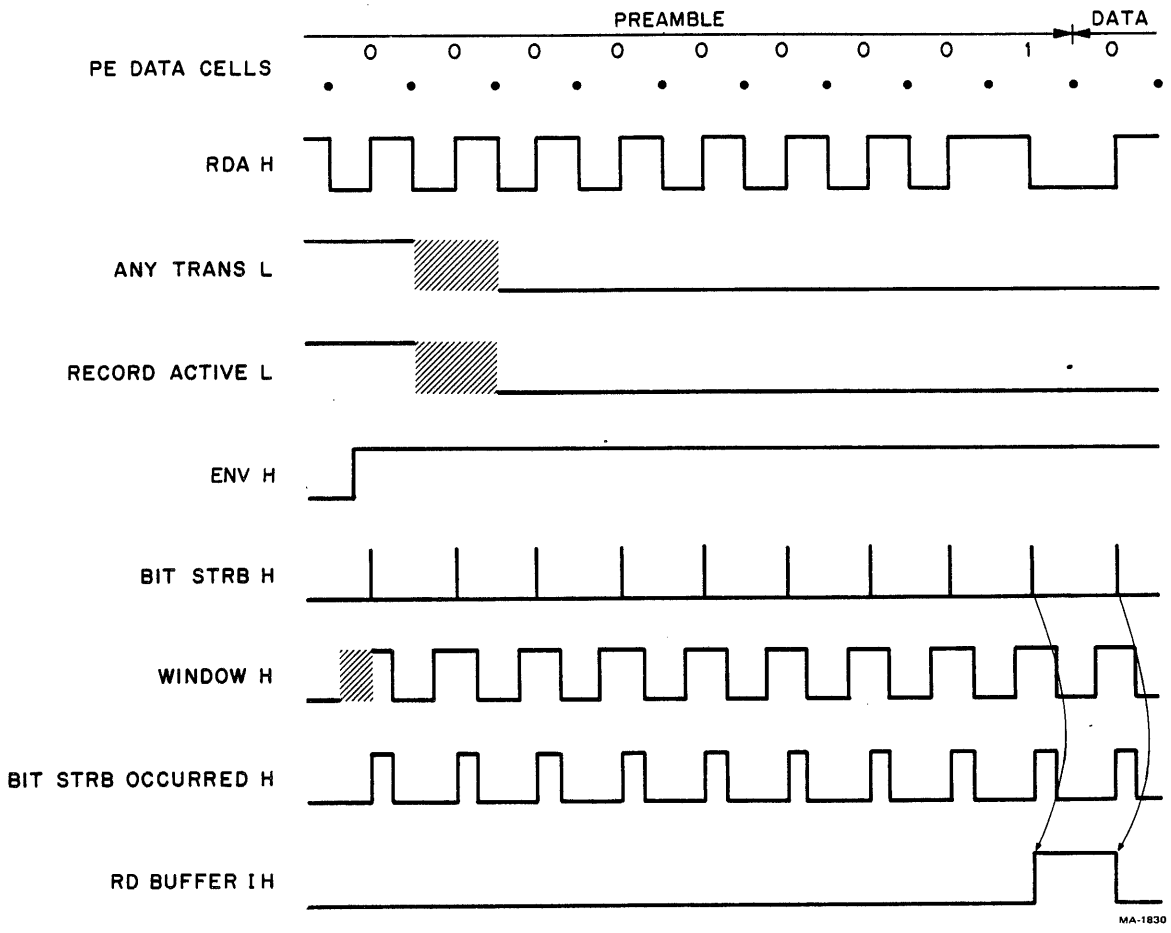


Figure 4-34 Data Discriminator Timing Diagram

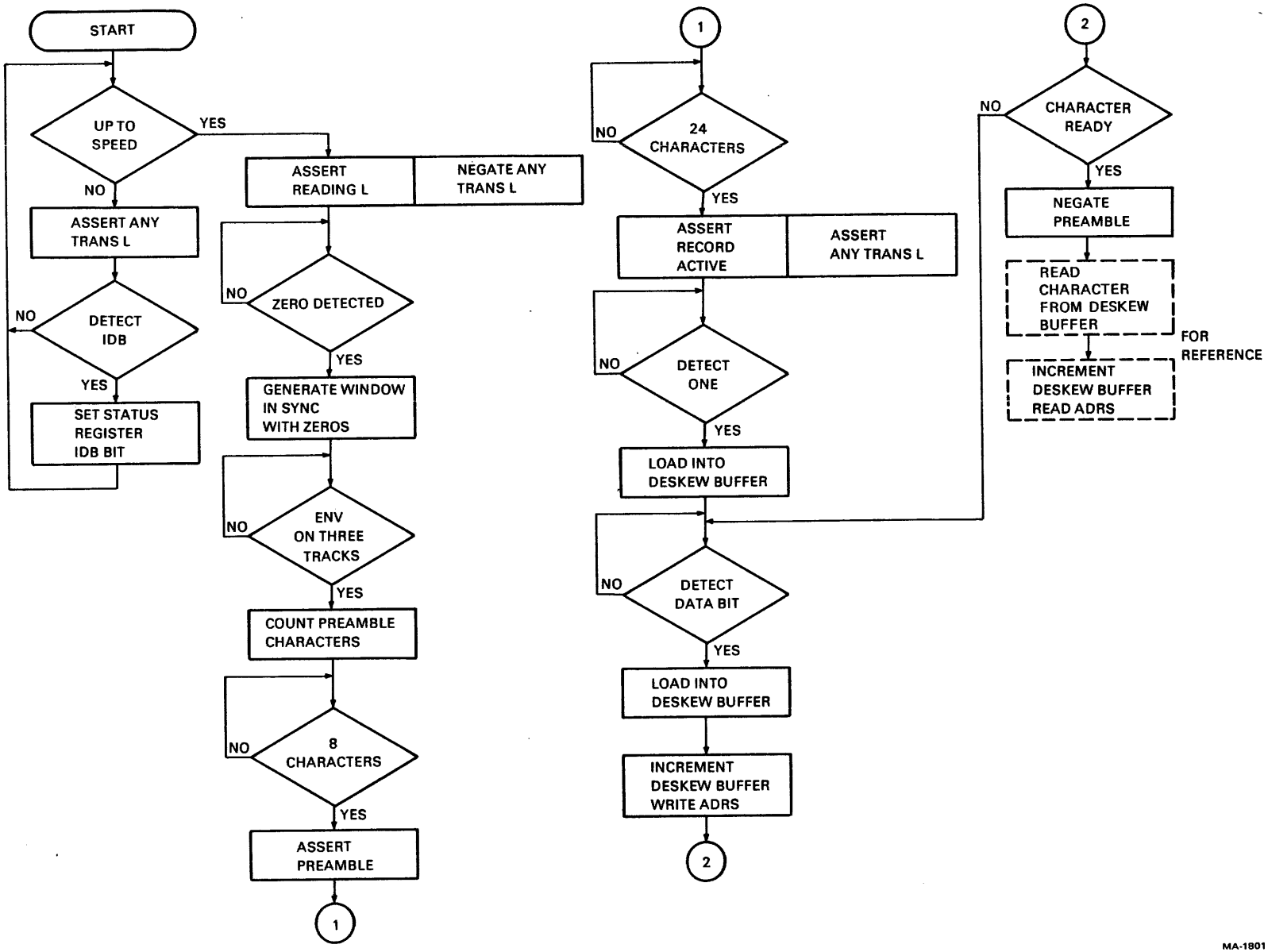


Figure 4-35 Preamble/IDB Detection Flowchart

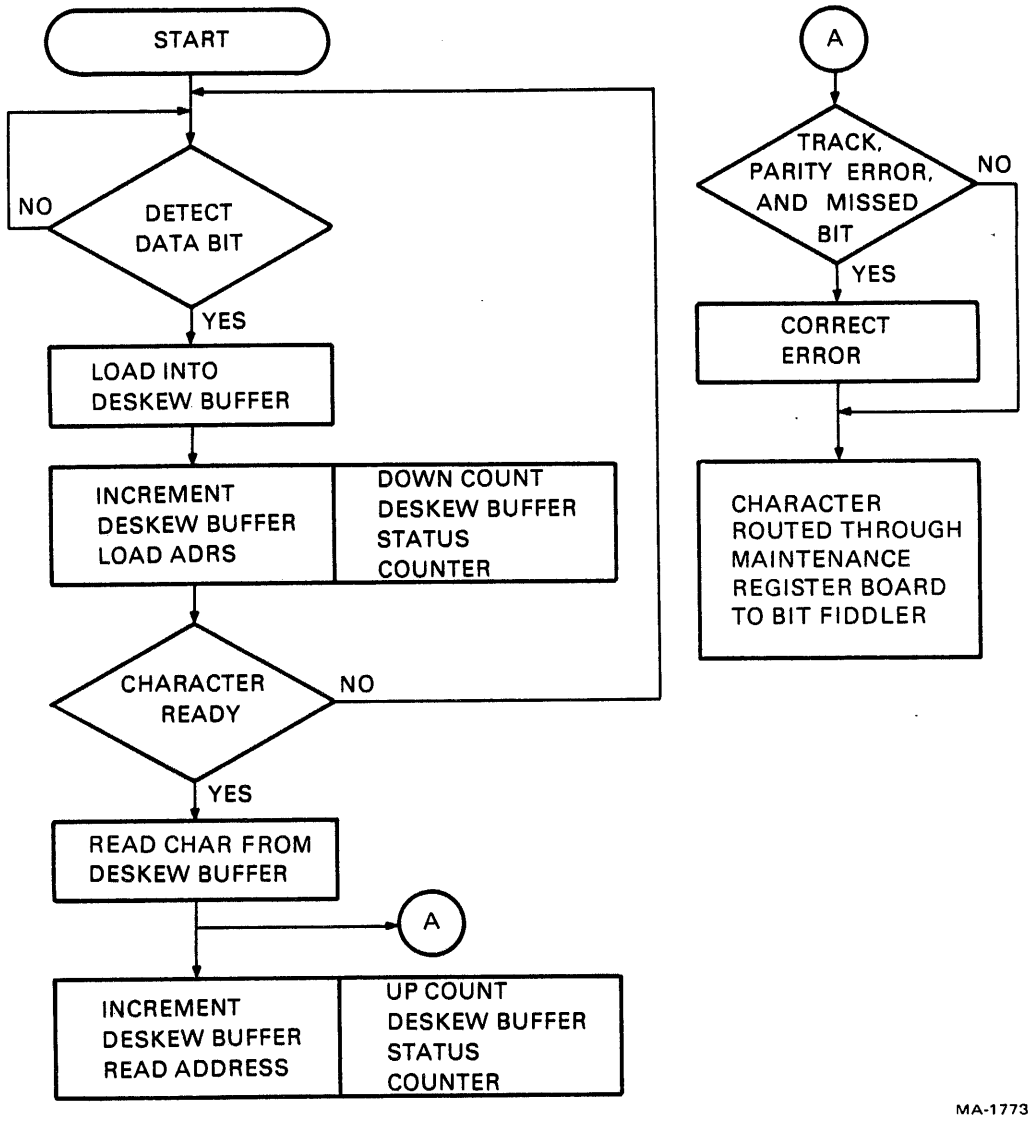


Figure 4-36 Data Sync Data Read Flowchart

With ONE DETECTED asserted, a counter (DS2) is enabled to determine deskew buffer status. Each time a data bit is loaded into the deskew buffer, the counter is decremented. Each time the deskew buffer is read, the count is incremented. Thus, the counter keeps track of how many unread data bits are in the deskew buffer.

When the nine deskew buffers contain an unread data bit, BIT READY H (common collectored) is asserted. BIT READY H causes CHAR SHIFT H and ENB RDS L to be asserted (TCPE3). CHAR SHIFT generates RD SYNC (0) H, which upcounts the deskew buffer status counters, thereby causing BIT READY H to be negated. CHAR SHIFT also increments the deskew buffer read address (TCPE4). ENB RDS L enables generation of RDS L by succeeding BIT READY H pulses. RDS L causes the output of the data sync modules (i.e., the contents of buffer B) to be read and assembled by the bit fiddler.

If skew of more than seven characters occurs during the read operation, the deskew buffer status counter of the leading track will be downcounted to seven, causing OVERFLOW L to be asserted. This sets the INC/VPE error bit in the error register. A skew of three or more characters causes the CS/ITM bit of the error register to be set.

Error Detection and Correction – If BIT STRB does not occur during any data cell, ENV H is negated and the DD TRK (dead track) flip-flop (DS3) is set. When the data of this data cell is read from the deskew buffer and loaded into buffer A, DROPPED BIT H will be generated as well. The outputs of buffer A of each track are input to a parity generator/checker (TCPE2). If there is only one dropped bit and a parity error is detected, PERR AND ONE DD TR H is generated; this means that the contents of buffer A of the dead track is of the wrong polarity. When the next CHAR SHIFT H is generated, this bit is corrected as it is clocked into buffer B; thus, on-the-fly error correction is achieved.

The outputs of buffer B are gated by PESB H (phase-encoded status buffered), and become RD B (read data B). The RD B lines are multiplexed in the maintenance register module and become RD C (read data C), and are then transmitted to the bit fiddler.

4.2.7.4 Postamble Detection – If on any track, a 1 bit followed by a 0 bit is read, POST PAT L is asserted (DS3). If this occurs simultaneously on all tracks, POST DETECT A,B,C H is asserted, and the postamble flip-flop (TCPE5) is set.

With the postamble flip-flop set, the character counter is further upcounted, and, when a count of 32 is reached (CT 5 H asserted), MID POSTAMBLE (1) is asserted. This signal loads the check character register (R07) with dead track information (MR4).

4.2.7.5 IRG Detection – If the transport read heads are passing over a portion of erased tape, no envelopes will be detected, and ANY ENV H will be negated. This also causes RS SHDN CNTR L (reset shutdown counter) to be negated (TCPE5), and allows the shutdown counter to be upcounted by 200 BPI CLK H. When a count of 15 is reached, EORS H and RECORD H are asserted. RECORD H indicates that an IRG is detected, while EORS H causes a stop motion delay to be generated.

4.2.7.6 IDB Detection – When the IDB is encountered, the parity read line contains alternate 1s and 0s; no other read lines transition.

The parity line (A RDA) is input to an XOR (DS2 and Figure 4-37) on the data sync module in slot C02. If tape is moving in the forward direction (REV L negated), A RDA is inverted. Thus, BIT STRB is of proper polarity for both forward and reverse tape motion.

The IDB detection circuitry produces a narrow pulse, BIT STRB H, each time the output of the bit strobe OR gate transitions. BIT STRB H sets ENV H. ENV H will remain asserted throughout the IDB.

During the IDB, the only track generating ENV H will be the parity track (track 4). This condition is recognized by circuitry on the tape control-PE module (TCPE4) and allows the IDB timer to be upcounted by 200 BPI CLK H. When the IDB timer reaches a count of 8, IDB H is asserted; this prevents further counting of the IDB timer, and asserts the IDB bit of the status register (R01).

4.2.7.7 Tape Mark Detection – A PE tape mark is defined as 0s in tracks 2, 5, and 8, while tracks 3, 6, and 9 are erased; or, as 0s in tracks 1, 4, and 7, while tracks 3, 6, and 9 are erased. This pattern is recognized in the TM03 by the generation of ENV H in tracks 2, 5, and 8 (or tracks 1, 4, and 7), while tracks 3, 6, and 9 do not generate ENV. When this condition is detected (TCPE4), FMK PATTERN is asserted, and the corresponding bit in the status register (R01) is set.

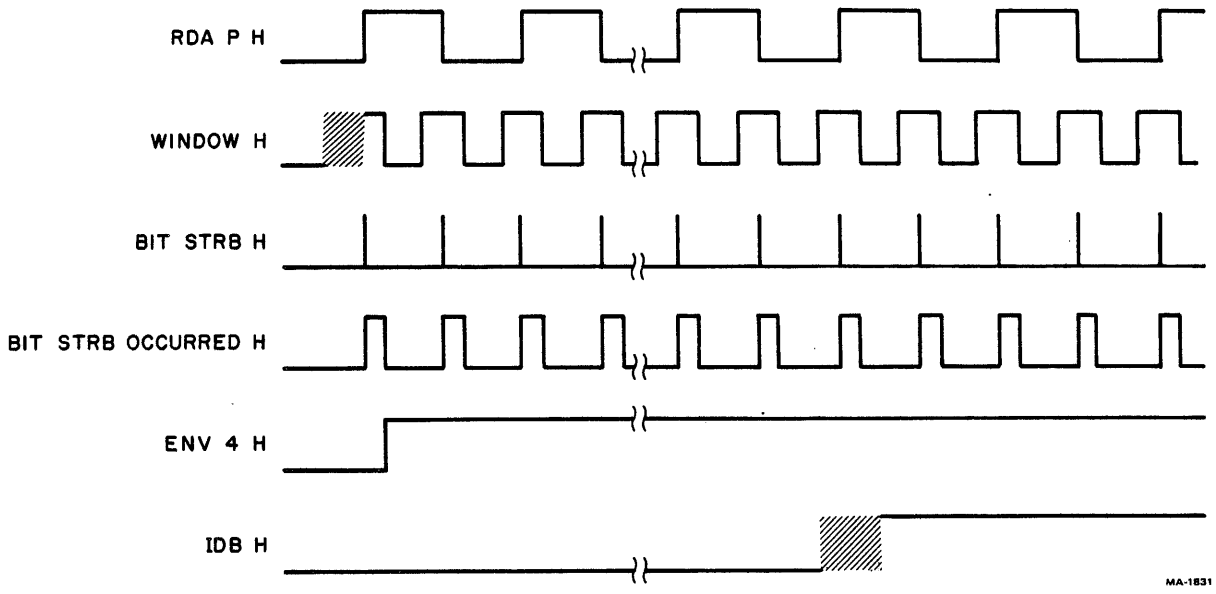


Figure 4-37 IDB Detection Timing Diagram

4.2.8 Read (NRZI)

This paragraph discusses the operation of the TM03 read circuitry when operating in NRZI mode. The NRZI read data path (Figure 4-4) is covered from the slave bus to the inputs of the bit fiddler. (Bit fiddler read operation is described in the latter paragraphs of this chapter.) The read data signals are received from the slave bus by the receiver terminator module (M8908-YA). The read data signals are then transmitted to the TCCM module in the TM03 where they are multiplexed to the tape control-NRZI module (M8934*).

4.2.8.1 Tape Control - Read Data Path - When RSDO is received in the tape control NRZI module, it is used to generate (CNRZ2) RD PLS, ERDS (enable read strobe), and RDS (read strobe). RD PLS loads the NRZI read latch (CNRZ4) with the tape character (RDA) from the TCCM module. The read latch outputs are then applied to nine XOR gates where, if necessary, error correction is performed. The read data (RDB) is then coupled to the maintenance register module where it is multiplexed to the bit fiddler. ERDS clocks the read LRC register and CRC generator (CNRZ4). Thus, a longitudinal parity check character and a cyclic redundancy check character are developed as data is read. This is discussed in more detail in Paragraphs 4.2.8.2 and 4.2.8.4.

4.2.8.2 CRCC Generation and Read - The read CRCC generator is clocked at the start of an operation by DRV SET PLS H. The register is then clocked by ERDS H each time a tape character is read, and the read CRCC is thus developed. Just before the CRCC is read from tape, the register should already contain the CRCC. It should therefore be cleared when the CRCC is read from tape; if not, a CRC error has occurred. When a CRC error occurs, COR/CRC L is asserted and the corresponding bit is set in the error register.

During a reverse read, when the second RDS H pulse is produced, REV CRCS L is asserted. During a forward read, FWD CRCS L is asserted when a binary counter reaches a count of three; this occurs three character cells after the last data character has been read.

REV CRCS L or FWD CRCS L generate CHK CHAR L. The negative-going edge of this signal clocks the check character register (R07) with the CRCC just read from tape.

4.2.8.3 NRZI Error Correction - A functional description of NRZI error correction, along with a flow diagram, is given in Paragraph 2.4. This paragraph provides a more detailed discussion of the three error correction cycles defined in Paragraph 2.4. The discussion follows a cycle flow diagram (Figure 4-38) of the error correction process. Figure 4-39 is a functional block diagram that complements the flow diagram.

NOTE

The functional block diagram, Figure 4-39, uses logical AND and OR symbols. It does not necessarily follow that a corresponding gate exists on the TM03 logic prints. The assertion of inputs A and B causing the assertion of output C may be represented on a block diagram by a single AND gate, yet the engineering drawing may show that several circuit stages are involved in the ANDing operation.

The signal names used on the functional block diagram are the names used on the engineering circuit schematics (CS prints). Where other signal names or notes are used, they are enclosed in parentheses.

*M8934-YA when used with a 190.5 cm/s (75 in/s) transport (TU45).

Cycle 1 – Cycle 1 consists of reading a record in the forward direction and sensing that there is a CRC error. Each RSDO pulse generates a RD PLS pulse, an ERDS pulse, and a RDS pulse. ERDS lags RD PLS by the duration of the ERDS one-shot (Figure 4-39, sheet 1). Data characters RDA0–RDA7, RDAP received from the TCCM module are latched up in the read latch register by RD PLS. The output of the read latch register is coupled through nine XOR gates and appears as RD0–RD7, RDP to the CRC forward/reverse register. If the operation being performed is a forward read, the data characters are output from the register in normal order, i.e., CRC (0–7, P), throughout the body of the record. If the operation being performed is a reverse read, REV CRCE ENBL is true and causes the register output to be in reverse order, i.e., CRC (P, 7–0). The data characters from the forward/reverse register are clocked into the CRC generator by ERDS. An error pattern register is also clocked by ERDS, thereby forming a pattern of the record being read. A vertical redundancy check (VRC) input to the error pattern register asserts whenever the character being input has a vertical parity error. Thus the error pattern accumulated is a function of both the number of characters in the record and those characters that have parity errors. The assertion of FWD LRCS signifies that all the data characters and the CRC character have been input to the CRC generator. Hence, FWD LRCS is used to inhibit further clocking of the generator and the error pattern register. If the record read was free of errors the output of the CRC generator (CRC ERROR) will be false and the TM03 will proceed to the next record. If one or more errors occurred in the record, CRC ERROR will be true. The next ERDS pulse will set the CRC error flip-flop and the cycle 1 flip-flop, thereby asserting CRC and CYCLE 1.

If a reverse read operation is being performed, the first character read is the LRC character. Thus REV LRCS is true, preventing the CRC generator and the error pattern register from being clocked, and the flow returns for the next input character, which is the CRC character. REV LRCS is now false and ERDS pulses clock the CRC character and the following data characters into the CRC generator until all the characters have been read and EOR asserts. If the record was free of errors, the output of the CRC generator (CRC ERROR) will be false and the TM03 will proceed to the next record. If one or more errors occurred in the record, CRC ERROR will assert and set the CRC error flip-flop, thereby asserting CRC. The cycle 1 flip-flop will not be set due to the reverse direction. The program must change to forward read and re-read the faulty record. Cycle 1 will then be entered via the forward read algorithm just described.

During normal operation, jumper W1 is not installed. If W1 is installed, the cycle 1 flip-flop is inhibited and the NRZI error correction capability is disabled.

Cycle 2 – Having entered cycle 1 in the forward direction, the program must now change to the reverse direction to enter cycle 2. If the transport is still in the forward mode when the next DRV SET PLS occurs, the cycle 1 flip-flop will be reset and the error correction process will abort. If REV is true when DRV SET PLS occurs, the cycle 2 flip-flop is set and CYCLE 2 asserts. Cycle 2 consists of computing the track in error.

The assertion of CYCLE 2 causes the following to occur.

1. The character inputs to the CRC generator are inhibited.
2. CRC data is gated from the CRC generator to the error pattern register.
3. ERDS pulses are inhibited from clocking the CRC generator and the error pattern register.

The CRC data from the CRC generator is compared with the error pattern in the error pattern register. The results of the comparison (EPR MATCH) gate ERDS pulses, which clock a track-in-error counter. The counter output is applied to a track-in-error decoder. The error decoder asserts one of ten outputs according to a 4-bit code received from the error counter. If a match is not obtained in the error pattern register, ERDS generates a CYCLE 2 CLOCK pulse, which increments the error counter and clocks the CRC generator. Clocking the CRC generator shifts the CRC data coupled to the pattern register and another attempt is made to obtain an EPR match. ERDS pulses continue shifting the data in the CRC generator and incrementing the track-in-error counter until an EPR match is obtained. When a match occurs, the CYCLE 2 CLOCK pulses are inhibited and the asserted output of the track-in-error decoder indicates the erroneous data track. If the error counter reaches a count of 9 (9 COUNT) and an EPR match was not obtained, the error is determined to be incorrectable and the error decoder asserts INC ERROR. The assertion of 9 COUNT inhibits any further clocking of the error counter.

If the reverse mode used for cycle 2 was reverse read, the program must reverse read one record and then change to forward read in order to enter cycle 3. The next DRV SET PLS resets the cycle 1 and cycle 2 flip-flops and, if the TM03 is in the forward read mode, sets the cycle 3 flip-flop. If the TM03 is not in the forward read mode, the error correction process is aborted.

If the reverse mode used for cycle 2 was reverse space, the program can reverse space any number (N) of records desired but then must forward space for N - 1 records to bring the faulty record up to the read heads. The program must now change to forward read in order to enter cycle 3. The next DRV SET PLS resets the cycle 2 flip-flop and, if the TM03 is in the forward read mode, sets the cycle 3 flip-flop. If the TM03 is not in the forward read mode, the error correction process is aborted.

Cycle 3 - Cycle 3 consists of re-reading the faulty record and correcting those characters that contain vertical parity errors. The characters from the read latch-up register are applied to nine XOR gates before being output to the maintenance register module. The XOR gates transfer input to output with no change, provided the second XOR inputs are negated. Cycle 3 functions to assert the second XOR input of the read line corresponding to the track in error for those characters with vertical parity error.

The characters from the read latch-up register are applied to a parity checker which asserts READ PAR ODD if good parity is obtained on the input character. If the checker detects a parity error, READ PAR ODD negates, causing VRC to assert. VRC true enables nine AND gates, one of which receives the asserted TRK "X" ERR from the error decoder (X = track number). The AND gate thus enabled asserts an input to its associated XOR gate in the read data path, thereby complementing the data bit of the track in error. If INC ERROR is true, there is no asserted TRK "X" ERR signal and the erroneous read data passes on unchanged.

When the CRC character is clocked into the read latch register, it too is checked for vertical parity error and, if necessary, corrected. A property of the CRC character is that it has odd parity if the number of data characters in the record is even, and even parity if the number of data characters is odd. An odd/even flip-flop is reset by the GO bit and toggled each time a data character is clocked into the read latch-up register. If the record contains an odd number of data characters, the flip-flop is in the set state at CRCS time; conversely an even number of data characters would leave the flip-flop in the reset state at CRCS time. The flip-flop output is XORed with READ PAR ODD. If the two XOR inputs are not alike (a 0 and a 1), the CRC character has good parity. (See Table 4-6 for the conditions prevailing when the CRC character has no parity error.) If the two XOR inputs are alike (both 0s or both 1s), the CRC character has a parity error. Like inputs cause the XOR output to negate, thereby asserting VRC. When VRC asserts, the CRC character is corrected by complementing the bit corresponding to the track-in-error in the same manner used to correct erroneous data characters.

Table 4-6 Conditions Prevailing When CRC Character Has No Parity Error

No. of data characters in record	1	2	3	4	5	6
State of odd/even flip-flop	1	0	1	0	1	0
Parity of CRC character	Even	Odd	Even	Odd	Even	Odd
READ PAR ODD	0	1	0	1	0	1
VRC	0	0	0	0	0	0

After the CRC character has been read, FWD LRCS asserts, enabling the CRC error flip-flop. If the error was uncorrectable, CRC ERROR will be asserted by the CRC generator and set the CRC error flip-flop just as in cycle 1. However, the true state of CYCLE 3 inhibits the setting of the cycle 1 flip-flop and prevents the TM03 from re-initiating cycle 1. The program will now initiate retry or other corrective procedures.

If the error was correctable, the GO bit resets the cycle 3 flip-flop, completing the error correction process.

Slave Address Change (SAC) – A SAC signal asserts whenever a new slave is selected, and negates when DRV SET PLS is asserted to the new slave. A SAC comparator compares the slave select bits from the tape control register with the output of a slave select register. The comparator asserts SAC when the two inputs do not agree. Thus SAC comes true when the select bits from the tape control register change and goes false when the next DRV SET PLS clocks the new select code into the slave select register. Should a new slave be selected during an error correction operation, SAC would reset the cycle 1 and cycle 2 flip-flops and the operation would abort. If the operation is already into cycle 3, the error correction will be completed before the new slave is addressed.

4.2.8.4 LRCC Generation and Read – The LRC check register (CNRZ4) is cleared at the start of an operation by DRV SET PLS H. The register is then clocked by ERDS each time a tape character is read. Each time a one-bit is read on a track, the corresponding bit in the register is toggled. Therefore, just before the LRC tape character is read, the register should contain the LRCC. When the LRC tape character is read, the register should contain all 0s; if it does not, an LRC error has occurred. The LRC check register output is ORed with CYCLE 3 and asserts LRCC MATCH when a good LRC is obtained on a character. LRCC MATCH is forced true by CYCLE 3 during the error correction process. (LRC error indications are inhibited in cycle 3 because the TM03 is already in the error correction process.) If an LRC error exists, LRCC MATCH is false and causes the PEF/LRC flip-flop to be set, thereby setting the corresponding bit in the error register. Note that during a reverse read the PEF/LRC flip-flop (CNRZ2) cannot be set due to the negated state of FWD LRCS. Thus the LRCC is ignored during a reverse read.

Because the LRCC is the last character read in a record, it is preserved in the data field of the maintenance register (R03). It can therefore be checked by performing a register read of R03.

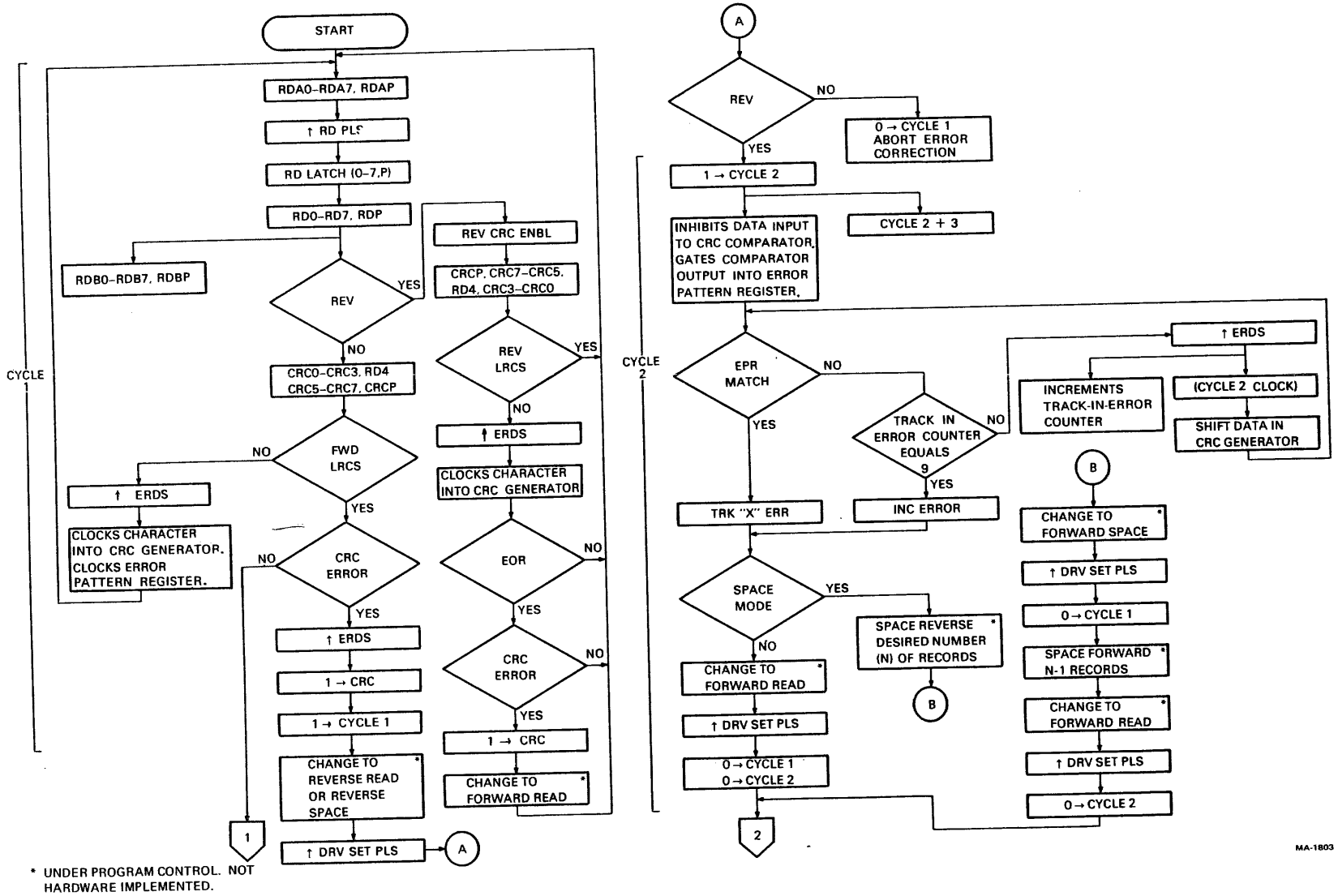


Figure 4-38 NRZI Error Correction Cycle Flow Diagram (Sheet 1 of 2)

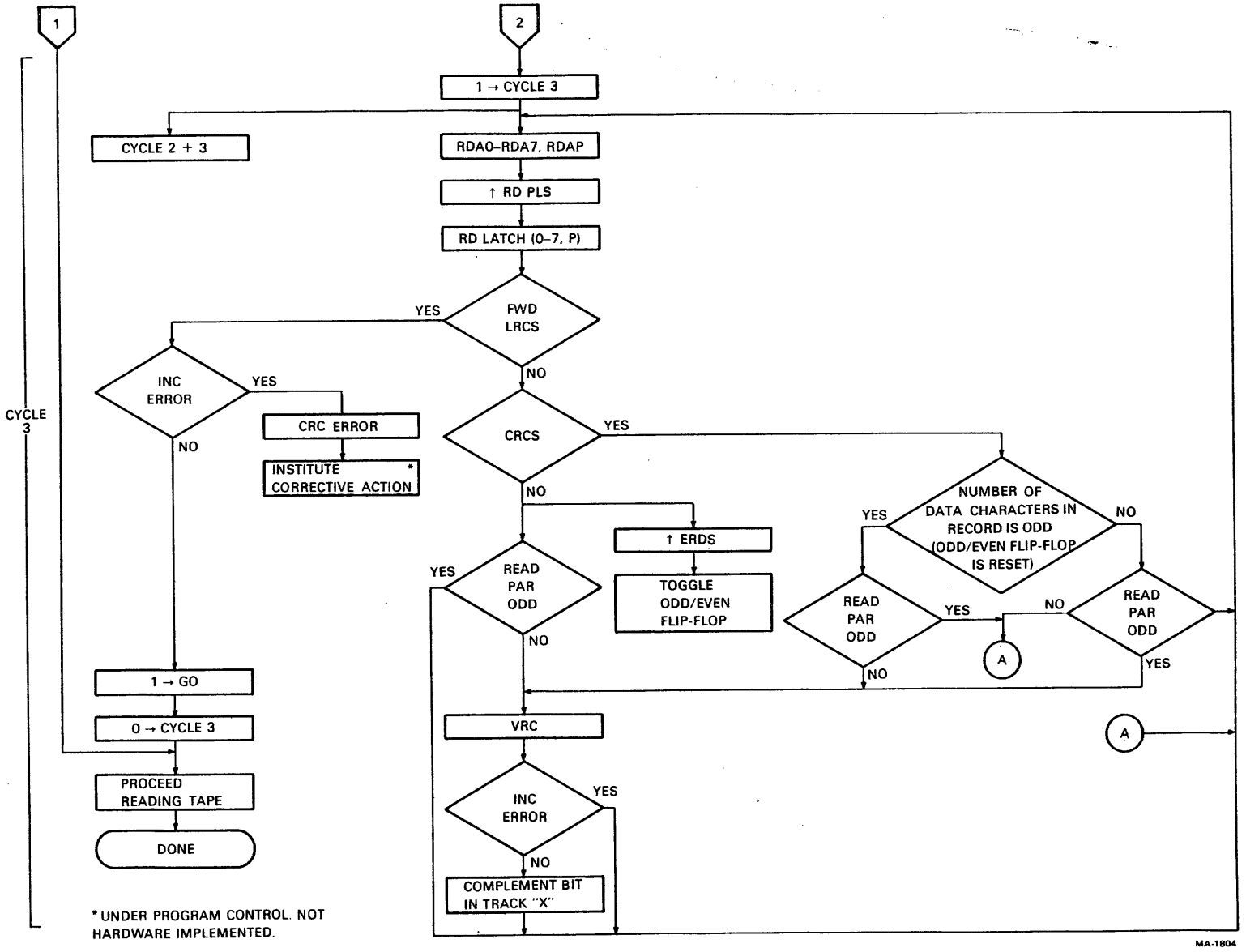


Figure 4-38 NRZI Error Correction Cycle Flow Diagram (Sheet 2 of 2)

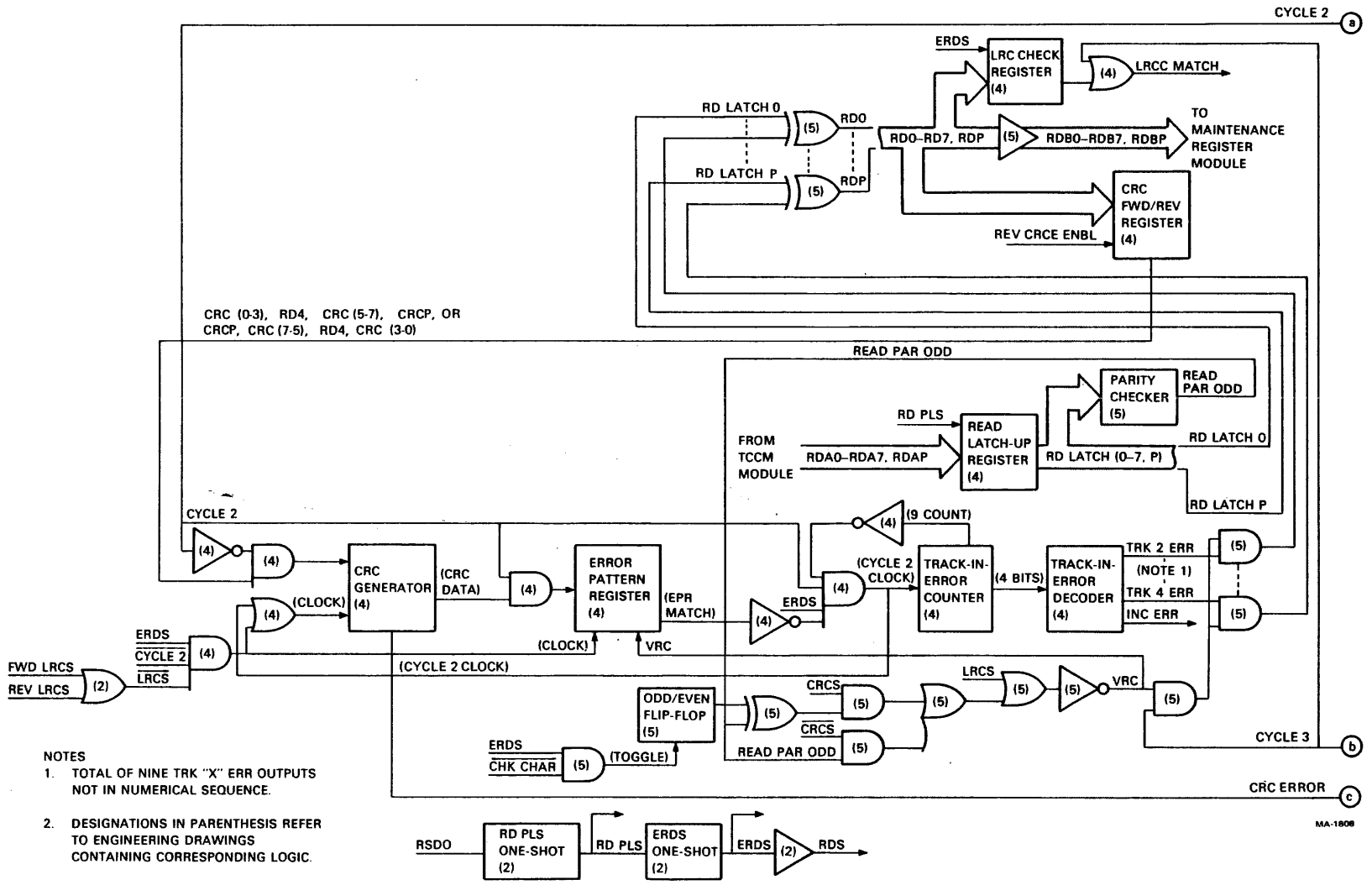


Figure 4-39 NRZI Error Correction Block Diagram (Sheet 1 of 2)

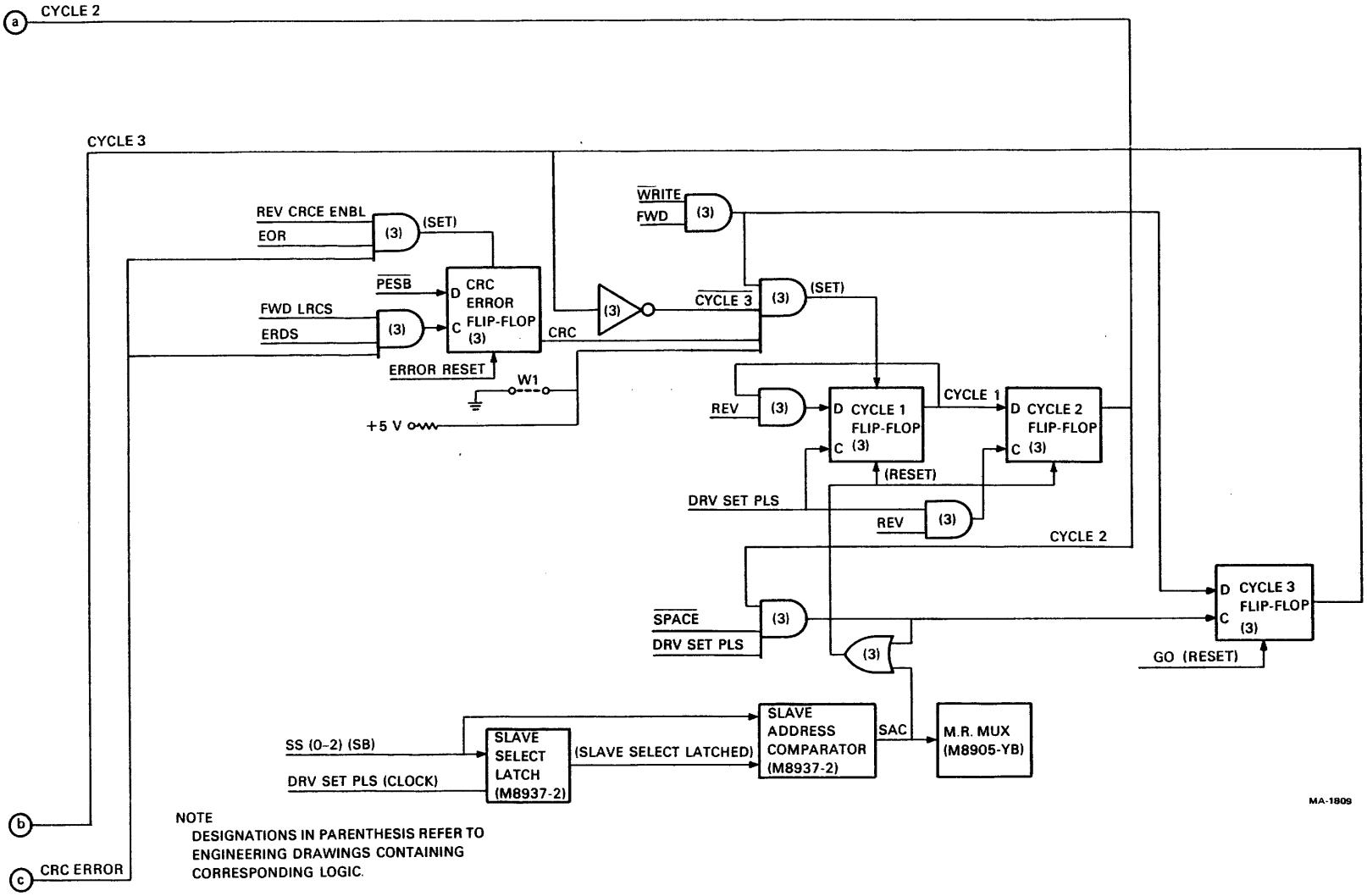


Figure 4-39 NRZI Error Correction Block Diagram (Sheet 2 of 2)

4.2.8.5 IRG Detection - As data is read from the tape, RSDO pulses are transmitted from the slave transport to the TM03 and cause the assertion of RST SHDWN CNTR L. RST SHDWN CNTR L (CNRZ4) constantly keeps resetting the shutdown counter (TCCM5). If RSDO pulses terminate, the shutdown counter is enabled for counting by 200 BPI CLK H. [During a write operation, the gap detection timer (TCCM5) must first time out before the shutdown counter is enabled.] When the shutdown counter reaches a count of 15, EORS H and RECORD H are asserted. EORS H causes a stop tape motion delay to be generated. RECORD H signifies that IRG has been detected.

If a write operation is in progress (IRG detected in a read-after-write sequence), and if data is detected after a count of SHDN = 8 and before the stop motion delay, a nonstandard gap error (NSG) is generated and the corresponding bit in the error register is set.

4.2.8.6 Tape Mark Detection - A set of two isolated characters, separated from each other by six to eight character lengths of erased tape, is recognized as an NRZI tape mark by the TM03. Refer to the NRZI tape mark detection logic (CNRZ1). The short record flip-flops were initially cleared by READING H negated during the start motion delay. As the read heads pass over the IRG, an RSDO H pulse sets the tape mark window flip-flop because NO CHAR RD L is asserted. The same RSDO pulse also sets the short record 1 flip-flop, which negates NO CHAR RD L and enables a binary counter to be upcounted by WRT CLK.

If the next RSDO H pulse occurs while the binary counter is at a count of 12 through 15, TPMK WINDOW (1) L will remain asserted. At the same time, SHORT REC I (1) H will be negated, and SHORT REC II (0) L will be asserted. These three conditions generate ENBL SHDN CNTR L. If no other characters are soon detected, the shutdown counter will assert SHDN = 8 H, which will cause the NRZI TMRK flip-flop to direct set.

The binary counter is preset to 6. Therefore, the tape mark is valid if the second character arrives six to eight character lengths after the first.

The TM03 will not read records of less than 10 characters. ENBL SHDN CNTR will not assert and enable a normal record shutdown until 10 RSDO pulses have occurred. Records under 10 characters are recognized as either a tape mark or assumed to be noise. By switching a jumper on the CNRZ module, the TM03 can be made to recognize records of less than 10 characters (minimum = 4). It should be noted that if this option is implemented, the probability of noise being mistaken for a record is increased (Paragraph 5.6.2.2).

4.2.9 Write (PE)

This paragraph discusses the operation of the TM03 write circuitry when operating in PE mode. The write data path (reference Figure 4-2) is covered from the output of the bit fiddler to the slave bus. Bit fiddler write operation is described in the latter paragraphs of this chapter.

4.2.9.1 PE Data Write - The characters multiplexed by the bit fiddler onto the write data bit fiddler output lines (WDBFO 0-7) are transmitted to the TCCM module. In the TCCM module, the WDBFO lines are applied to the A inputs of the TCCM write multiplexer (TCCM2) and multiplexed to the TCCM write buffer.

When the write buffer receives WB CLK H, it is loaded with the output of the write multiplexer. The complemented outputs of the write buffer are applied to the D inputs of the write multiplexer and loaded into the write buffer at alternate WB CLK H pulses. This operation phase encodes the binary data output of the bit fiddler.

The uncomplemented outputs of the TCCM write buffer are driven by drivers across the slave bus to the slave transport.

4.2.9.2 PE Data Write Timing – When the TM03 decodes a write data function code, it places the WRITE and FWD commands on the slave bus. When the Massbus controller asserts RUN, the TM03 generates DRV SET PLS, which sets the WDR (write data record) flip-flop (TCCM4); this enables generation of WB CLK and REC L pulses when WRT CLK is received from the slave transport. The TM03 also transmits SLAVE SET PLS to the slave transport.

When the transport is up to speed (ACCL H negated), the PE write major states circuitry (TCPE3) is enabled; at the same time, the slave begins to transmit WRT CLK to the TM03. The write major states circuitry enables the various segments of a PE data record (preamble 0s, preamble 1s, data, postamble 1s, and postamble 0s) to be written. While the preamble is being written, WRT CLK generates WB CLK and REC L pulses (TCCM4). WB CLK is used in the TCCM write circuitry (TCCM2) to phase encode the preamble (Figure 4-40). REC L is transmitted to the slave and causes the phase-encoded characters generated by the TCCM write buffer to be transferred to tape.

When the preamble has been written, the write major states circuitry asserts DATA H. This enables the generation of WRT STRB in addition to WB CLK and REC L, and changes the mode of the TCCM write multiplexer operation so that it gates data characters from the bit fiddler to the TCCM write buffer. The WRT STRB pulses cause the bit fiddler to generate tape characters from the data words it receives from the Massbus controller. WB CLK pulses clock the TCCM write buffer and phase encode the bit fiddler outputs, while the REC L pulses transmitted to the slave transport cause the data to be transferred to tape. The writing of the data portion of a PE record terminates with frame count register (R05) overflow.

4.2.9.3 Preamble Write Timing – The write major states circuitry on TCPE3 controls various stages of a PE write data operation. At the beginning of a write data operation in PE mode, WDR H (TCCM4) enables the PRE 0 flip-flop (TCPE3) to be clocked set by ST CLK (state clock). However, write major states circuitry operation is inhibited until the end of the start motion (acceleration) delay. When the start motion delay is over (ACCL negated), the PRE 0 flip-flop is set; PRE 0 asserts PE WRT ENB L. At the same time, WRT CLK pulses received by the TM03 produce PE CLK, WB CLK H, and REC L pulses (TCCM4). PE CLK and PESB (phase-encoded status buffered) cause the S0 and S1 inputs of the TCCM write multiplexer (TCCM2) to toggle as illustrated in Figure 4-40. Because ONES H is not asserted, phase-encoded 0s are loaded into the TCCM write buffer by WB CLK. (The operation is identical to the manner in which postamble 0s are produced, illustrated in Figure 4-40.)

The number of preamble 0s generated is counted by the motion delay counter on TCCM3. When forty 0s have been generated, FORTY H causes the PRE 0 flip-flop to be cleared and the PRE 1 flip-flop to be set; this asserts ONES L, causing the TCCM write buffer to be loaded with a phase-encoded 1s character. REC L pulses are continuously transmitted to the slave and cause the forty 0s and the 1s character to be transferred to tape.

After the preamble 1s character is written, the PRE 1 flip-flop is cleared, and the data flip-flop is set. DATA H asserted causes the data portion of the PE record to be written, as described in Paragraph 4.2.9.2.

4.2.9.4 Postamble Write Timing – When the frame count register overflows (indicating that the data has been written), WRITE END L is generated (MBI9) and clears the write data record flip-flop (TCCM4). WDR H negated clears the data flip-flop (TCPE3) and causes the POS 1 flip-flop to set. This asserts ONES L, and changes the mode of TCCM write multiplexer operation (Figure 4-40), so that a phase-encoded 1s character is generated and written on tape. The next ST CLK pulse clears the POS 1 flip-flop. This negates ONES L and enables the postamble 0s to be written on tape. The ST CLK pulse that follows sets the POS 0 flip-flop. While POS 0 is asserted, the binary counter on TCCM3 is upcounted from 40 to 80, during which time 40 postamble 0s are written on tape. When EIGHTY L is asserted, the POS 0 flip-flop is cleared; this completes the PE record.

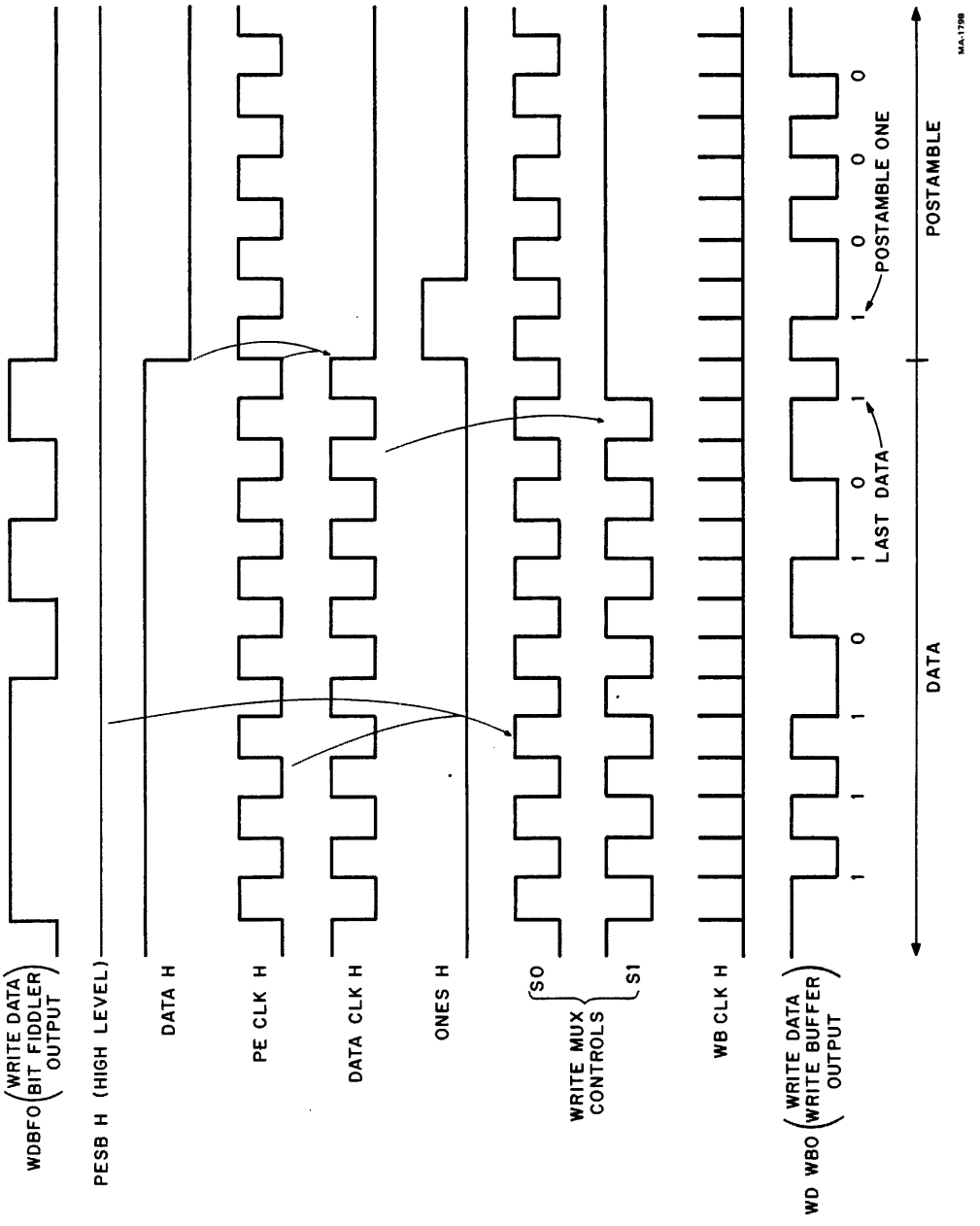


Figure 4-40 TCCM Write Operation Timing (PE)

4.2.9.5 PE Tape Mark Generation – When DRV SET PLS is produced, it causes the TMWIP (tape mark write in progress) flip-flop (TCCM4) to be set. When the start motion delay is over, the write major states circuitry (TCPE3) is enabled, and TMWIP H allows the PRE 0 flip-flop to set. This causes the assertion of PE WRT ENB L, which enables generation of PE CLK, WB CLK, and REC L pulses (TCCM4).

With PRE 0 asserted, almost the same situation exists as when preamble 0s are written (Paragraph 4.2.9.3). Forty tape characters will be written on tape. However, because WFMK L is asserted, bits 3, 4, and 6 of the TCCM write buffer are force cleared. Thus, instead of all-0 tape characters, only tracks 1, 2, 4, 5, 7, and 8 will contain 0s; tracks 3, 6, and 9 (corresponding to bits 3, 4, and 6) will be erased.

When the 40 characters comprising the tape mark have been written, FORTY H (TCCM3) causes the PRE 0 flip-flop (TCPE3) to be cleared; this inhibits further WB CLK and REC L pulses.

4.2.9.6 IDB Generation – The IDB is written on tape automatically when a slave transport operating in PE mode is commanded to perform a write operation while at BOT. The circuitry that detects this condition is located on the TCCM module (TCCM3). The count in the motion delay counter is used to activate the write IDB circuitry. During a write from BOT operation, the start motion delay is initiated. During the delay, the write IDB flip-flop is forced set and asserts WRT ID BURST L. The flip-flop remains set while the identification burst is written.

WRT ID BURST L asserted negates ACCL (SB) L; this enables the slave transport to transmit WRT CLK to the TM03. WRT ID BURST also generates PE WRT ENB L (TCPE3), which enables generation of PE CLK, WB CLK, and REC (TCCM4). At the same time, WRT ID BURST clears all the bits of the TCCM write buffer (TCCM2) except for the parity bit. WRT ID BURST H enables PARITY DATA SET UP H, which causes the write buffer parity bit to produce alternate 1s and 0s. The net result is alternate 1s and 0s on the parity track (track 4) while all other tracks are erased.

4.2.10 Write (NRZI)

This paragraph discusses the operation of the TM03 write circuitry when operating in NRZI mode. The write data path (reference Figure 4-2) is covered from the output of the bit fiddler to the slave bus. Bit fiddler write operation is described in the latter paragraphs of this chapter.

4.2.10.1 NRZI Data Write – The characters, multiplexed by the bit fiddler onto the write data bit fiddler output lines (WDBFO 0–7), are transmitted to the TCCM module. In the TCCM module, the WDBFO lines are applied to the A inputs of the TCCM write multiplexer (TCCM2) and multiplexed to the TCCM write buffer.

When the write buffer receives WB CLK H, it is loaded with the outputs of the write multiplexer. The outputs of the write buffer are then driven by drivers across the slave bus to the slave transport.

4.2.10.2 NRZI Data Write Timing – When the TM03 decodes a write data function code, it places the WRITE and FWD commands on the slave bus. When the Massbus controller asserts RUN, the TM03 generates DRV SET PLS, which sets the WDR (write data record) flip-flop (TCCM4); this enables generation of WB CLK and REC L pulses when WRT CLK is received from the slave transport. The TM03 also transmits SLAVE SET PLS to the slave transport.

When the transport is up to speed, WRT CLK pulses are transmitted to the TM03 and generate WRT STRB, WB CLK, and REC L pulses. WB CLK is used to load the TCCM write buffer with the outputs of the TCCM write multiplexer (Figure 4-41). REC L is transmitted by the TM03 to the slave transport where it causes the tape character presently in the TCCM write buffer to be transferred to tape. WRT STRB activates the bit fiddler to generate the next character.

WB CLK, WRT STRB, and REC L pulses continue until the WDR flip-flop is cleared. This occurs when the frame count register overflows and generates WRITE END (MBI9).

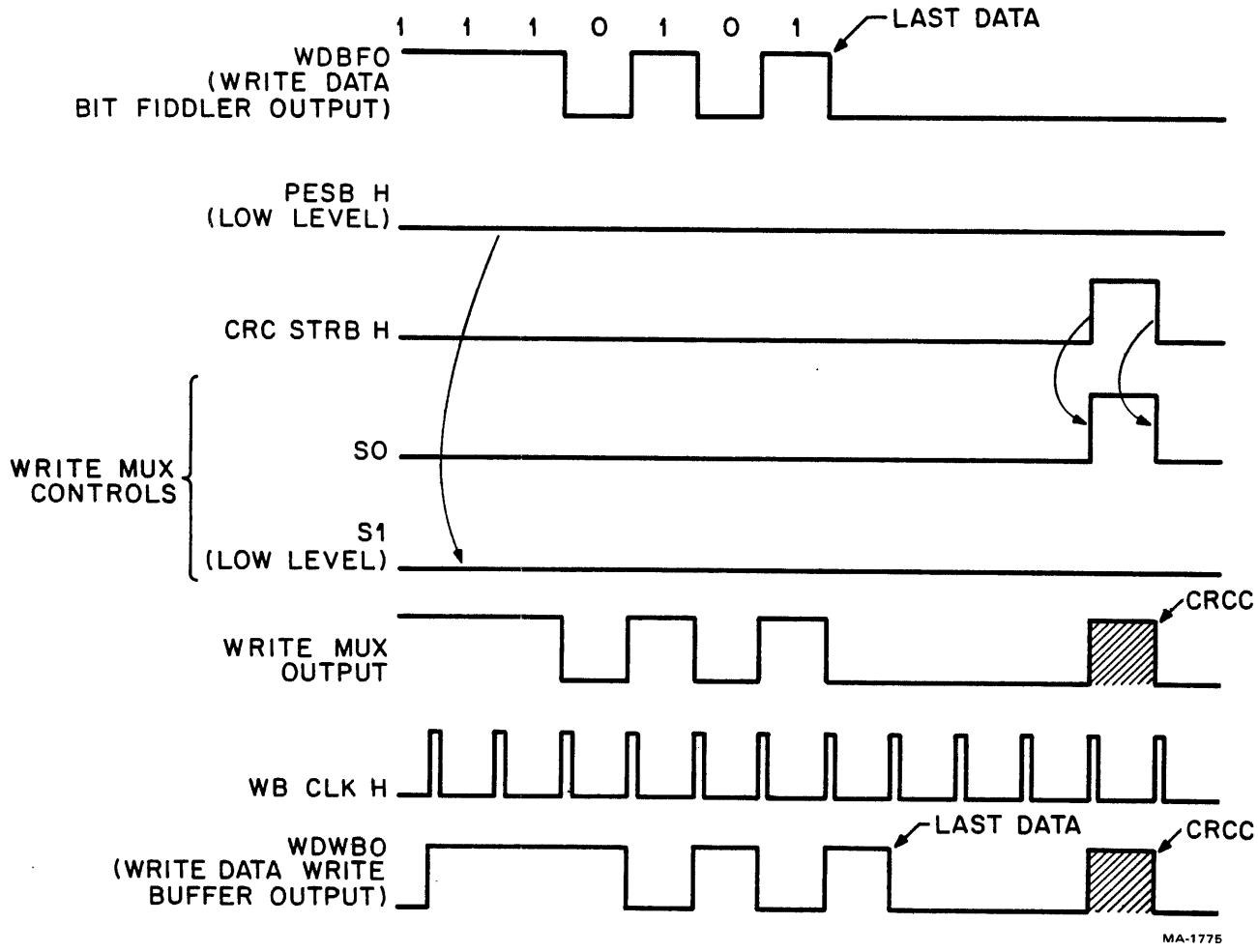


Figure 4-41 TCCM Write Operation Timing (NRZI, 1 of 9 tracks)

4.2.10.3 CRCC Generation - Data input to the TCCM is also input to the CRCC generator (CNRZ2). The generator, clocked by WB CLK, produces the CRCC by a series of shifts and XORs. The outputs of the CRCC generator (CRC 0-7, P) are applied to the B inputs of the TCCM write multiplexer. After the data portion of the record is written, the CRCC is transmitted to the slave transport and written on tape.

4.2.10.4 CRCC and LRCC Write Timing - When the data portion of an NRZI record has been written, the WDR flip-flop is cleared; this enables a binary counter* (TCCM4) to be upcounted by WRT CLK. The counter, initially preset to a count of 8, generates CRC STRB H when it reaches a count of 11, and LRC STRB L when it reaches a count of 15. At a count of zero, further clocking is inhibited. Therefore, three clock pulses increment the counter to 11; another four clock pulses increment it to 15, so that CRC STRB H is produced three character spaces after the data, and LRC STRB L is generated seven character spaces after the data (Figure 4-42).

*M8934 only. M8934-YA uses a shift register instead of a counter.

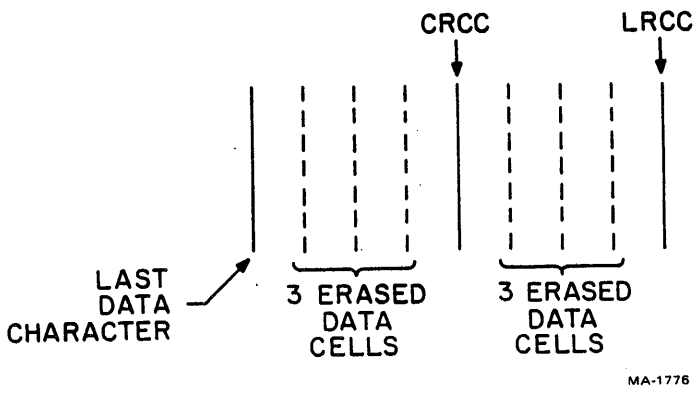


Figure 4-42 CRCC and LRCC Timing

Whenever LRC STRB or CRC STRB occur, WRT CLK ENBL H is momentarily asserted, and gates out one WB CLK H pulse and one REC L pulse.

When CRC STRB H is asserted, the TCCM write multiplexer (TCCM2) gates the output of the CRCC generator (CNRZ2) to the TCCM write buffer (Figure 4-41). The WB CLK produced at CRC STRB time loads the buffer with the CRCC. The character is then driven to the slave transport via the slave bus.

LRC STRB clears the entire TCCM write buffer (TCCM2) and causes 0s to be transmitted to the slave transport. LRC STRB is also transmitted to the slave transport.

4.2.10.5 NRZI Tape Mark Generation – During a write tape mark operation, WFMK is asserted. WFMK L causes all the bits of the TCCM write buffer (TCCM2) to be cleared, while at the same time NRZ WTMK L, 7CH TM1 and 7CH TM0 are generated. These signals are input to slave bus drivers thereby forcing the tape mark character onto the write data (WD) lines of the slave bus. The tape mark character forced on the WD lines is 23_8.

4.2.10.6 Tape Mark Write Timing – The assertion of DRV SET PLS causes the TMWIP (tape mark write in progress) flip-flop (TCCM4) to set. This loads a binary counter and allows WRT CLK H to be gated and produce WB CLK H and REC L.

When the start motion delay is over and the first WRT CLK pulse is received by the TM03, the first WB CLK H produced clears the TMWIP flip-flop; thus, further WB CLK and REC L pulses are temporarily inhibited. The REC L pulse produced, along with the WB CLK H pulse, cause the tape mark character to be transferred to tape.

With the TMWIP flip-flop now clear, the binary counter is enabled. It operates in the same manner as during a CRCC and LRCC write, except that WFMK H asserted (TCCM4) inhibits the production of CRC STRB H. However, LRC STRB is produced in the normal manner, and occurs seven character spaces after the tape mark character.

The LRC STRB L input to an AND gate on the TCCM module (TCCM2) removes the tape mark character forced onto the WD lines of the slave bus. LRC STRB L and the REC L pulse it produces are transmitted to the slave transport, thereby transferring the LRCC of the tape mark character (which is identical to the tape mark character) to tape.

4.2.11 Bit Fiddler - M8915-YA*

NOTE

The functional block diagrams in Paragraph 4.2.11 use logical AND and OR symbols. It does not necessarily follow that a corresponding gate exists on the TM03 logic prints. The assertion of inputs A and B causing the assertion of output C may be represented on a block diagram by a single AND gate, yet the engineering drawing may show that several circuit stages are involved in the ANDing operation.

The signal names used on the functional block diagrams are the names used on the engineering circuit schematics (CS prints). Where other signal names or notes are used they are enclosed in parentheses.

4.2.11.1 General - During a write operation the M8915-YA bit fiddler receives 16- or 18-bit data inputs from the Massbus and disassembles it into 8-bit tape characters for the tape transport. During a read operation, 8-bit tape characters received from the tape transport are reassembled into a 16- or 18-bit format and transferred out to the Massbus. The assembly/disassembly process is under the program control of a microcontroller ROM. The ROM senses the type of operation, direction of motion, and format specified by the system program and branches to the proper routine to perform the specified type of transfer. Parity checks are made on data into the M8915-YA, and parity is generated for data out of the M8915-YA, for both read and write operations. In addition, internal parity checks are made on the data during the assembly/disassembly process.

4.2.11.2 Data Transfer Formats (Figures 4-43, 4-44, and 4-45) - The assembly/disassembly process involves transferring the data in 4-bit groups or "nibbles." Figure 4-43 shows the 18 Massbus data bits and five 4-bit groups labeled A through E. The A, B, C, and D bit groupings are different in the upper SET LEFT format than in the lower SET RIGHT format. For example, group A in the SET LEFT format contains Massbus bits 17 through 14 while group A in the SET RIGHT format contains bits 15 through 12. Groups A through D are transferred as 4-bit groups while group E is transferred as either a 4-bit group or as two 2-bit groups designated as E LEFT and E RIGHT. Groups F and G are 4-bit groups that make up the 8-bit tape character.

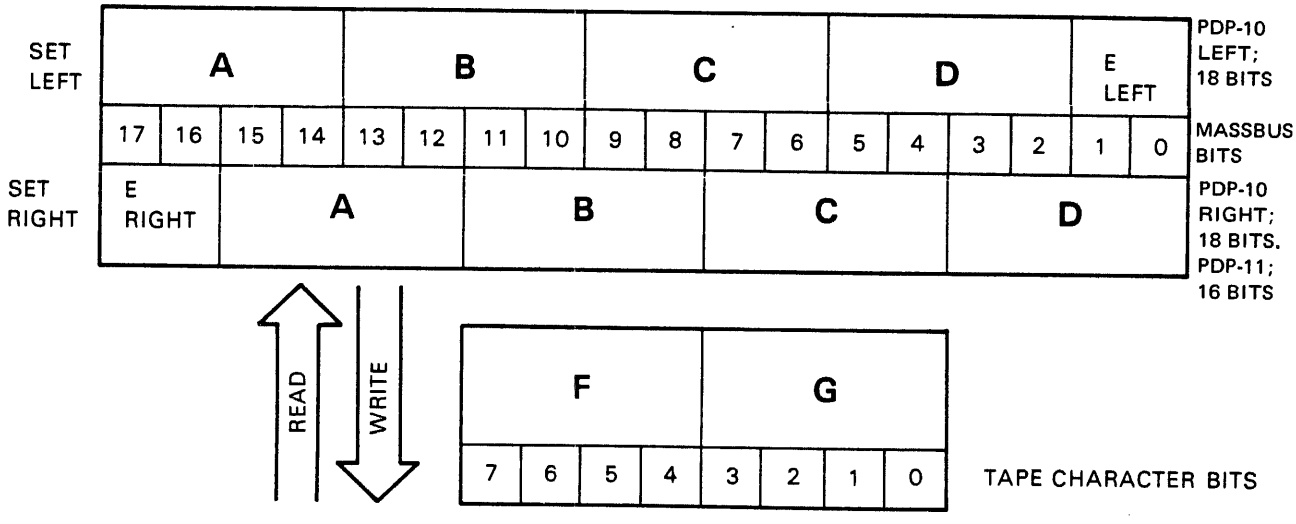


Figure 4-43 Massbus to Tape Character Disassembly/Assembly

*TE16 and TU45 can also use M8915. The TU77 [317.5 cm/s (125 in/s)] must use the M8915-YA.

A 16-bit PDP-11 word is completely contained within four nibbles. Therefore SET RIGHT is the only format used for PDP-11 operations. During a PDP-11 write operation, nibbles C and D are transferred to F and G, to form a tape character. Then nibbles A and B are transferred to F and G forming another tape character, thus writing the entire PDP-11 word on tape. During a PDP-11 read forward operation, the reverse process occurs. A tape character is placed into groups F and G and transferred to groups C and D. The next tape character is also placed into F and G and transferred to A and B. Groups A, B, C, and D are then placed onto the Massbus in bits 15 through 00. (Massbus bits 16 and 17 are not used for PDP-11 operations.)

PDP-15 format operations are identical to PDP-11 format operations except for the order of group transfers (Figure 4-44). Bits 00 and 01 of the PDP-15 data word (corresponding to Massbus bits 16 and 17) are ignored.

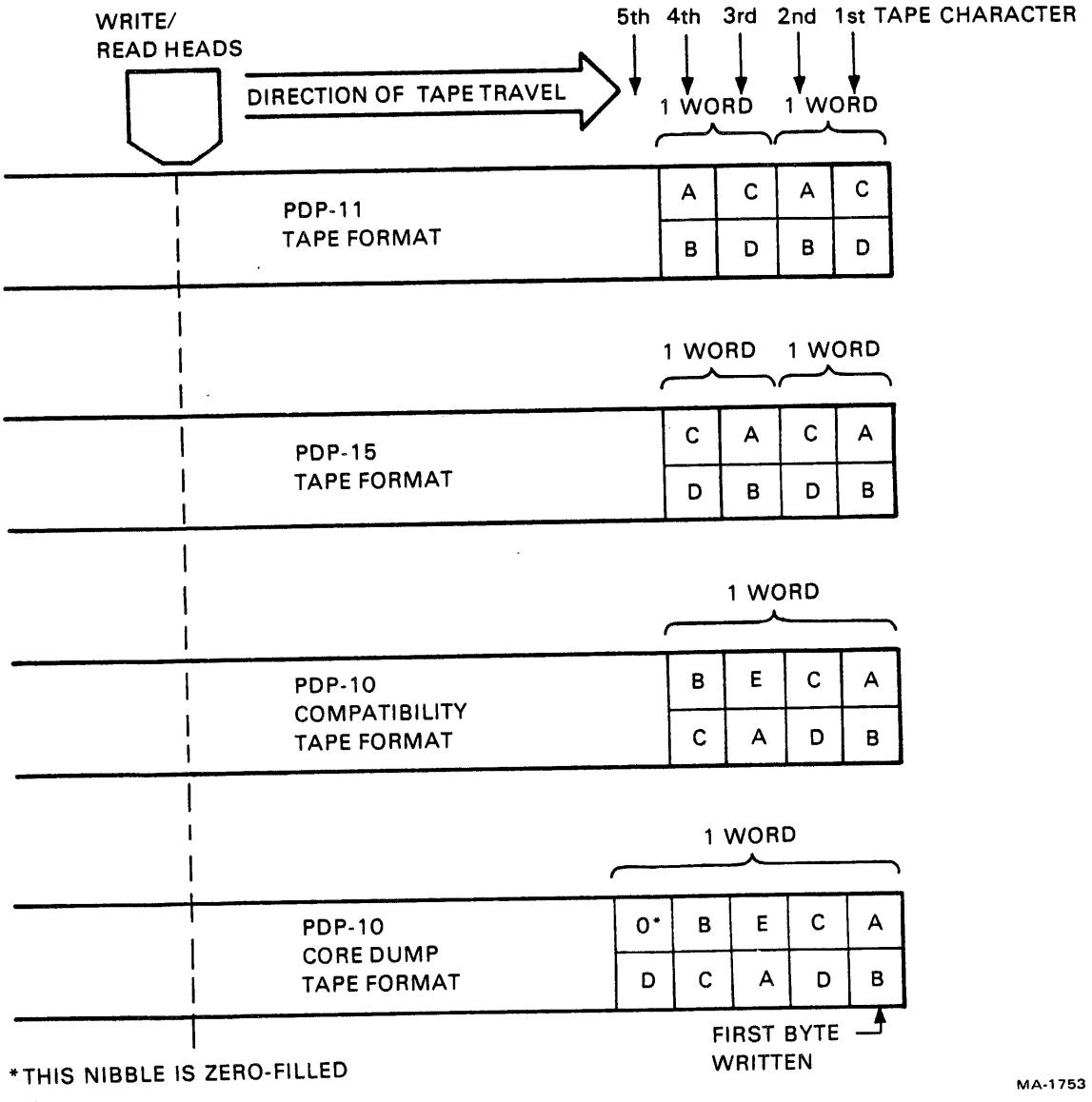


Figure 4-44 Tape Recording Formats

Figure 4-45 illustrates the formats for PDP-10, PDP-15, and PDP-11 data words and how they are placed on the Massbus for processor/Massbus transfers. All three formats place the most significant bits in the high numbered bit locations on the Massbus. In the PDP-11 format, bit 0 is the LSB while bit 0 is the MSB in the other formats.

The format for disassembling a 36-bit PDP-10 word and transferring it to tape is more complex. The disassembly process uses both the SET LEFT and SET RIGHT formats and all five of the 4-bit data groups. The first half of the PDP-10 word is received on the Massbus as bits 17–00 and the SET LEFT format is used. Groups A and B are transferred to F and G for the first tape character and groups C and D are transferred to F and G for the second tape character. Bits 01 and 00 are placed into the E LEFT half of group E. The second half of the PDP-10 word is received on the Massbus as bits 17–00 and the SET RIGHT format is used. In the SET RIGHT format, bits 17 and 16 are placed into the E RIGHT half of group E. Groups E and A are now transferred to F and G for the third tape character. Note that this character contains 2 bits from the first 18 data bits received on the Massbus. Groups B and C are then transferred to F and G for the fourth tape character. Bits 3–0 (group D) still remain to be written on tape. In the PDP-10-compatible mode, these bits are ignored and the process is repeated for the next PDP-10 word. In the PDP-10 core dump mode, the four bits in group D are written on tape as a fifth tape character. Group D is transferred to group G and group F is zero-filled.

During a PDP-10 read forward operation, the process is reversed. The first tape character is placed into groups F and G and transferred to A and B in the SET LEFT format. The second tape character is placed into F and G and transferred to C and D. The third tape character is placed into F and G but only group F is transferred to group E, and only the E LEFT half of group E is placed onto the Massbus. After the 18-bit Massbus output has been transmitted, the SET RIGHT format is asserted. The E RIGHT half of group E already has data from group F of the third tape character. The second half of the third tape character (group G) is then transferred to group A. Then the fourth tape character is placed into F and G and transferred to B and C. In the read PDP-10 compatible mode, the D group is zero-filled and the second 18-bit Massbus output is transmitted to complete the reading of a 36-bit PDP-10 word. In the read PDP-10 core dump mode, a fifth tape character is read from tape into group F and G. Group G is transferred to D and the 18-bit Massbus output is transmitted. (Group F contains all zeros as this nibble was zero-filled during the core dump write operation.)

4.2.11.3 2907 Data Latches (Figure 4-46) – The grouping of four bits into data nibbles is accomplished by 2907 latches composed of eight D-type flip-flops. The latches are labeled A through G and correspond to groups A through G discussed in Paragraph 4.2.11.2. Four of the flip-flops receive the input nibble and the other four flip-flops transmit the output nibble. The outputs of the receive flip-flops are gated to a 4-line bidirectional data bus (D0–D3) by MC "X" TO BUS. The bus also provides the inputs to the four transmit flip-flops. When MC BUS TO "X" asserts, the bus data is clocked into the transmit flip-flops, which output the data nibble.

Each latch generates a parity bit for the nibble clocked into the receive side and the nibble clocked out of the transmit side. The signal MC "X" TO BUS selects one of these for the DR P "X" parity bit for the latch. When MC "X" TO BUS is true, DR P "X" is the parity bit for the input nibble. When MC "X" TO BUS is false, DR P "X" is the parity bit for the output nibble.

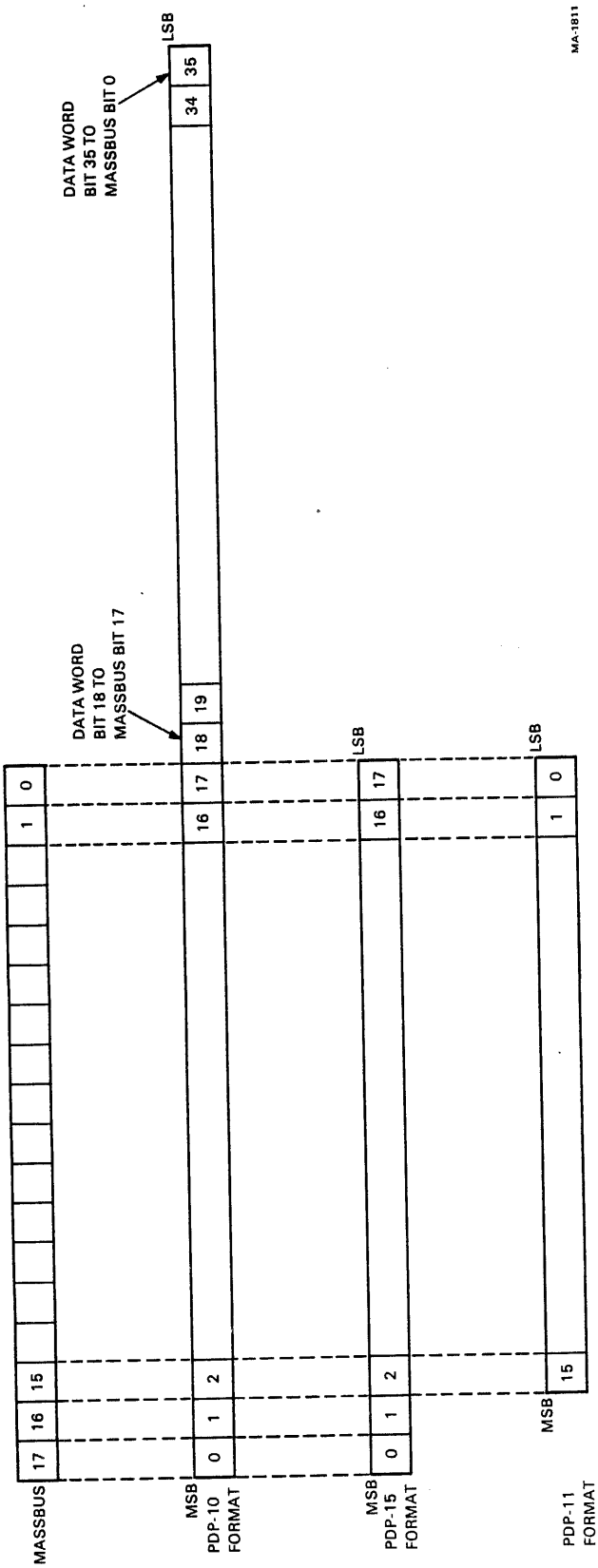


Figure 4-45 Processor Data Word Formats on Massbus

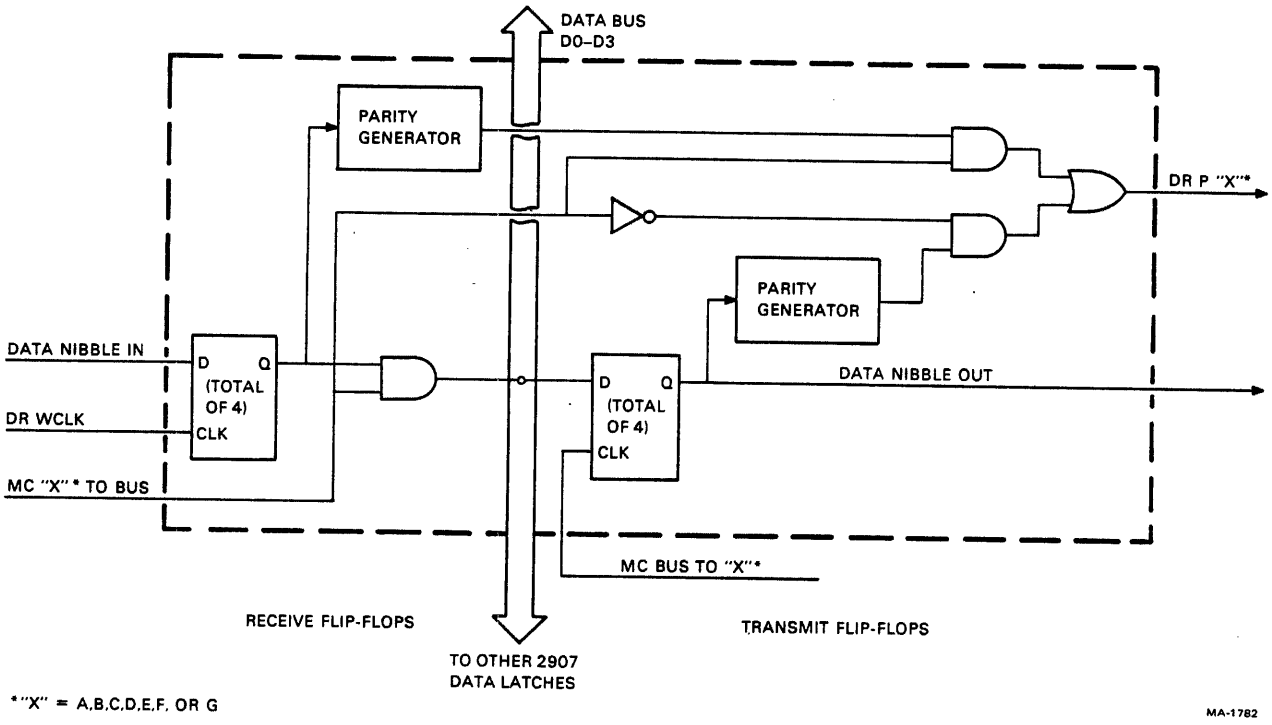


Figure 4-46 2907 Latch Logic

4.2.11.4 Write Data Path (Figure 4-47) - The 18-bit data word (MB D17 REC - MB D00 REC) is taken from the Massbus, via the Massbus receivers, and clocked into the left/right input multiplexer by WCLK. The multiplexer disassembles the 18-bit input into 4-bit nibbles and distributes the nibbles to latches A through E. The distribution varies according to whether an MC SET LEFT format or an MC SET RIGHT format is asserted. The distribution for both formats is shown in Figure 4-43. The trailing edge of WCLK clocks the nibble into the five latches. Note that different clock signals are applied to each half of the E latch. Bits 01 and 00 are clocked into latch E left by DR GET LEFT during a SET LEFT, and bits 17 and 16 are clocked into latch E right by DR GET RIGHT during a SET RIGHT.

The 4-line data bus carries the nibbles from latches A through E to latches F and G where the 8-bit tape characters are assembled. The assertion of MC A TO BUS by the program places the nibble in latch A onto the data bus. The assertion of MC BUS TO F by the program clocks the nibble into the transmit flip-flops of latch F. The program then negates MC A TO BUS and MC BUS TO F, and asserts MC B TO BUS and MC BUS TO G, thereby transferring the nibble in latch B to the transmit flip-flops of latch G. The TCCM or tape control NRZI module takes the 8-bit tape character from latches F and G, after which the program repeats the sequence for the other nibbles. Thus each nibble gets placed onto the data bus and transferred to latch F or G. When latches F and G are full, they are output to the TCCM or tape control NRZI module as a tape character to be written, and the process is repeated.

When a write operation calls for a zero-fill into latch F,* MC BUS TO "X" is asserted to latch F without a corresponding MC "X" TO BUS asserted to latch A, B, C, D, or E. This results in all zeros being clocked into latch F due to the data bus terminators.

4.2.11.5 Read Data Path (Figure 4-47) - An 8-bit tape character (RDC0–RDC7) received from the maintenance register module is clocked into latches F and G by RDS (read strobe). The assertion of MC F TO BUS by the program places the nibble in latch F onto the data bus. The assertion of MC BUS TO A by the program clocks the nibble into the transmit flip-flops of latch A. The program then negates MC F TO BUS and MC BUS TO A and asserts MC G TO BUS and MC BUS TO B, thereby transferring the nibble in latch G to the transmit flip-flops of latch B. The next RDS pulse clocks the next tape character into latches F and G and the process is repeated. Thus each tape character is clocked into latches F and G, placed on the 4-bit data bus as data nibbles, and transferred to latches A through E.

The left/right ouput multiplexer accomplishes the reverse of the left/right input multiplexer. It takes the nibbles in latches A through E and assembles them into an 18-bit data output for the Massbus. The 20 bits from latches A through E are applied to the output multiplexer which selects 18 of the 20 bits for output to the Massbus. Only two of the bits from latch E are used for each 18-bit output. All four bits from latches A through D are used for each output but their position on the Massbus varies according to whether a SET LEFT format or a SET RIGHT format is asserted. Figure 4-43 shows how the four bits from each latch are positioned on the Massbus for the SET LEFT format and the SET RIGHT format. Note that during a SET LEFT the two bits from latch E left are used, and during a SET RIGHT the two bits from latch E right are used.

The assertion of MC SET SCLK clocks the data into the multiplexer, thereby transferring it to the Massbus as D17 TM - D00 TM. After the assertion of MC SET SCLK, latches A through E start filling up with new data nibbles and the process is repeated.

*A write zero-fill is done only in PDP-10 core dump operation, and then only into latch F.

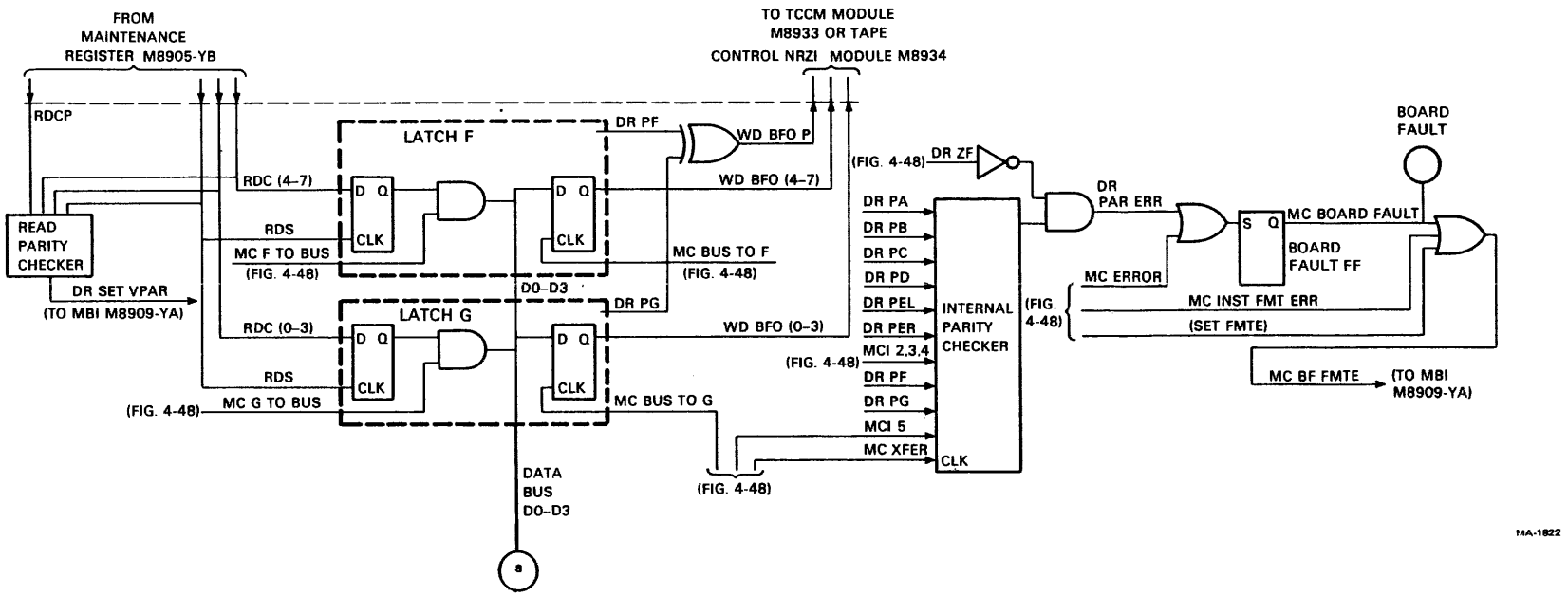


Figure 4-47 Write/Read Data Paths (Sheet 1 of 2)

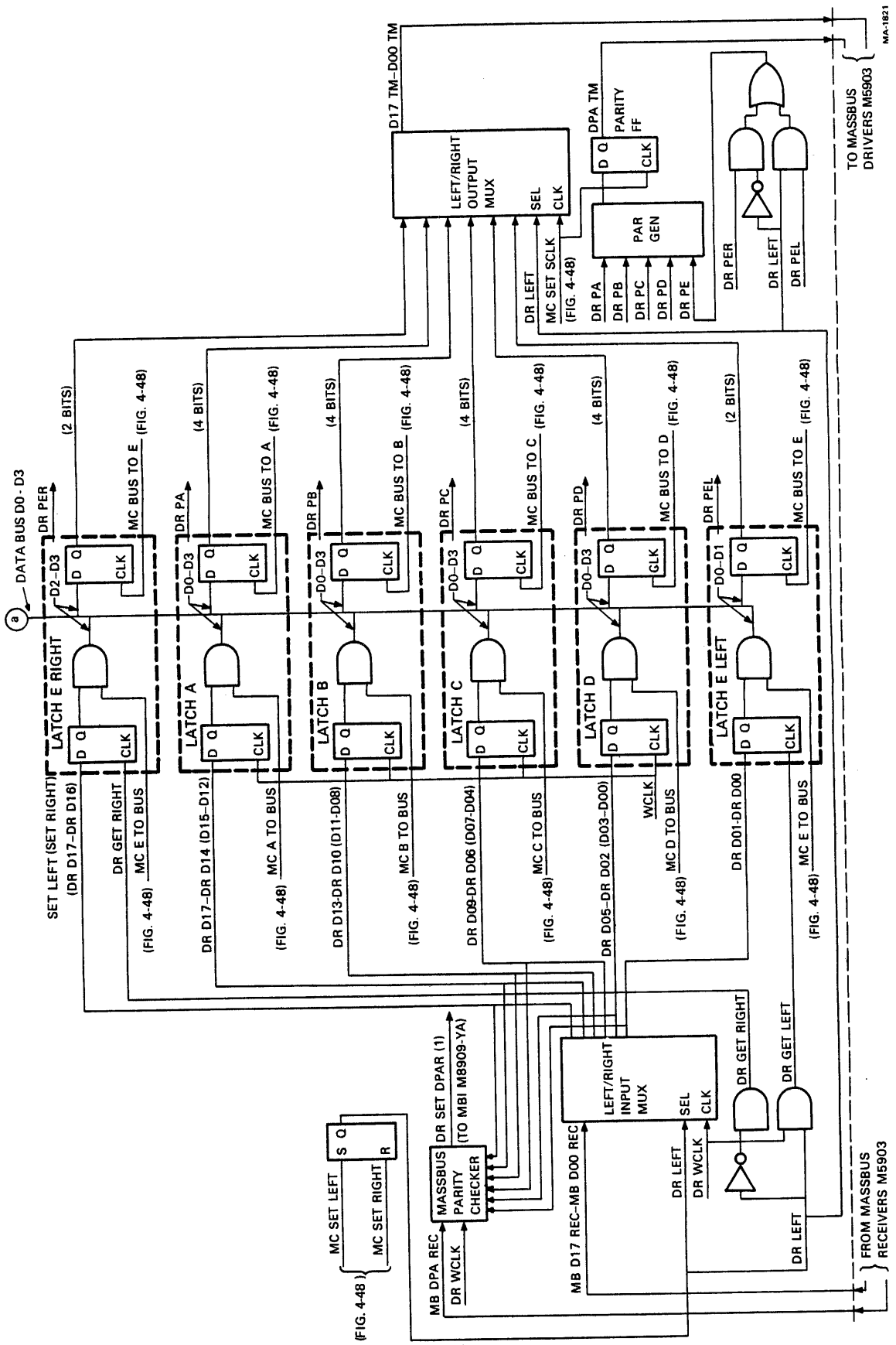


Figure 4-47 Write/Read Data Paths (Sheet 2 of 2)

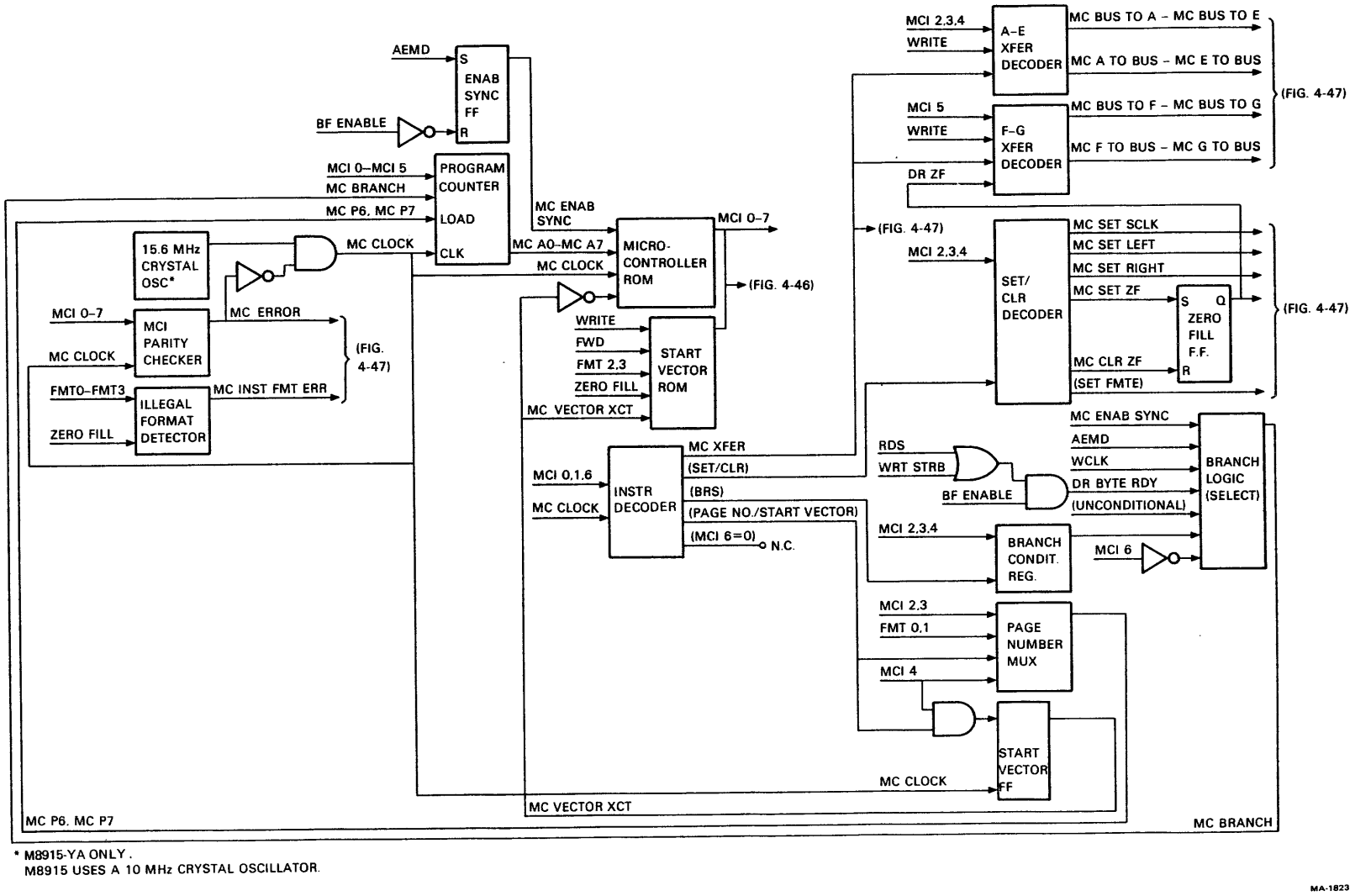
When a read operation calls for a zero-fill into latch A, B, C, D, or E, MC BUS TO "X" is asserted to the latch without a corresponding MC "X" TO BUS asserted to latch F or G. This results in all zeros being clocked into the latch due to the data bus terminators.

4.2.11.6 Data Parity - Data parity is checked when data is input to the bit fiddler and internally during the assembly/disassembly process. Parity is generated for the data output from the bit fiddler.

During a write operation, the data clocked into the left/right input multiplexer is checked in a Massbus parity checker. If an error is detected, DR SET DPAR (1) is asserted and sent to the error register in the MBI module. As the data is being disassembled, parity is checked on each nibble transferred from latches A through E to latches F or G. The A through E latch involved in a transfer will have its MC "X" TO BUS asserted, thereby outputting DR P "X" for the nibble being placed on the data bus (Figure 4-46). The F or G latch involved in the transfer will have its MC "X" TO BUS negated, thereby outputting DR P "X" for the nibble being taken from the data bus. These two parity bits are compared in an internal parity checker which asserts DR PAR ERR if a match is not obtained (provided the transfer is not a zero-fill). Microcode instruction MCI2, 3, 4 (discussed in Paragraph 4.2.11.7) selects the A through E latch involved in the transfer, and MCI5 selects the F or G latch involved. DR PF and DR PG are exclusive-ORed to generate the parity bit WD BFO P for the output tape character.

During a read operation the tape character input to latches F and G is checked in a read parity checker. If an error is detected, DR SET VPAR is asserted and sent to the error register in the MBI module. As the data is being assembled, parity is checked on each nibble transferred from latches F or G to latches A through E. The F or G latch involved in a transfer will have its MC "X" TO BUS asserted, thereby outputting DR P "X" for the nibble being placed on the data bus. The A through E latch involved in the transfer will have its MC "X" TO BUS negated, thereby outputting DR P "X" for the nibble being taken from the data bus. These two parity bits are compared in the internal parity checker, which asserts DR PAR ERR if a match is not obtained and the transfer is not a zero-fill. Microcode instruction MCI2, 3, 4 selects the A through E latch involved in the transfer and MCI5 selects the F or G latch involved. The parity bits from latches A through E are applied to a parity generator whose output is applied to a parity flip-flop. When MC SET SCLK is asserted, the flip-flop outputs the parity bit to the Massbus. At the time MC SET SCLK asserts, the DR P "X" bit from each latch is the parity of the output nibble being applied to the output multiplexer. Note that the DR PE bit will be from latch E left when MC SET LEFT is true, and from latch E right when MC SET RIGHT is true.

4.2.11.7 Program Control (Figure 4-48) - Operation of the bit fiddler is controlled by a microcontroller ROM (control ROM) which outputs 8-bit microcode instruction words. The instruction words (MCI0–MCI7) specify the instruction to be performed and the instruction parameters. A binary program counter is incremented by MC CLOCK and supplies the address inputs (MC A0 - MC A7) to the control ROM. During system startup, the MC ENAB SYNC input to the control ROM is false, causing the ROM program to loop on itself in an idle mode. As the tape transport comes up to speed, BF ENABLE and AEMD assert, setting the ENAB SYNC flip-flop and asserting MC ENAB SYNC. The assertion of MC ENAB SYNC takes the ROM program out of the idle mode and initiates a GO routine wherein the program determines the type of operation to be performed.



* M8915-YA ONLY.
M8915 USES A 10 MHz CRYSTAL OSCILLATOR.

Figure 4-48 Bit Fiddler Program Control Block Diagram

A second ROM (start vector) also outputs MCI0–MCI7 in parallel with the control ROM output. The normally negated state of MC VECTOR XCT inhibits the start ROM and enables the control ROM, thus allowing the instruction words from the control ROM to operate the bit fiddler. During the control ROM GO routine, MC VECTOR XCT is asserted and transfers control to the start ROM for one instruction. The only type of instruction the start ROM issues is a branch instruction, which causes the control ROM program to branch to the starting address of 1 of 12 operational routines. The routines that may be selected are listed below:

11	Write Forward Normal	10	Write Forward, Core Dump
11	Read Forward Normal	10	Read Forward, Core Dump
11	Read Reverse Normal	10	Read Reverse, Core Dump
11	Write Forward (PDP-15 – Normal)	10	Write Forward, Compatible
11	Read Forward (PDP-15 – Normal)	10	Read Forward, Compatible
11	Read Reverse (PDP-15 – Normal)	10	Read Reverse, Compatible

The routine addressed by the start ROM is determined by ROM inputs WRITE, FWD, FMT2, and FMT3 (ZERO FILL is not used). The start ROM forces a branch to the selected routine by asserting MC BRANCH and loading MCI0–MCI5 into the program counter. Address inputs MC P6 and MC P7 are obtained from the page number multiplexer and reflect the state of format bits FMT0 and FMT1. This will be discussed later in this section. After the routine's starting address is loaded into the program counter, MC VECTOR XCT negates and program control returns to the control ROM. The program counter then steps the control ROM through the routine which executes the selected type of data transfer.

Bits MCI0, 1, 6 are input to the instruction decoder and specify the instruction to be executed. On the next assertion of MC CLOCK, the decoder outputs the selected instruction (MC XFER, SET/CLR, BRS, or PAGE NO./START VECTOR).

When the instruction decoder asserts the MC XFER instruction, the A-E XFER decoder and the F-G XFER decoder are enabled. The A-E XFER decoder outputs MC "X" TO BUS if WRITE is true or MC BUS TO "X" if WRITE is false. "X" will be A, B, C, D, or E as determined by MCI2, 3, 4 of the XFER instruction word. The F-G XFER decoder will output MC BUS TO "X" if WRITE is true or MC "X" TO BUS if WRITE is false. "X" is either F or G as determined by MCI5 of the XFER instruction word.

When the instruction decoder asserts the SET/CLR instruction, the SET/CLR decoder is enabled and outputs MC SET SCLK, MC SET LEFT, MC SET RIGHT, MC SET ZF (zero fill), or MC CLR ZF as determined by MCI2, 3, and 4 of the SET/CLR instruction word. A sixth output, SET FMTE (set format error), asserts if an attempt is made to execute an illegal operation. This output is not asserted during normal operation. It signifies an error condition and is discussed under program errors, Paragraph 4.2.11.8.

When the instruction decoder asserts the BRS (branch condition select) instruction, the MCI2, 3, 4 bits of the BRS instruction word are latched into the branch condition register. The register output is applied to the branch logic where it selects either the unconditional state or one of four input signals (MC ENAB SYNC, AEMD, WCLK, or DR BYTE RDY) for monitoring. When the MCI6 input to the branch logic is false, MC BRANCH asserts if the selected branch condition is met. Any instruction word with MCI6 negated is a branch instruction with MCI0–MCI5 of the instruction word being the branch address. (Note that when MCI6 is negated, there is no instruction output from the instruction decoder.) If the branch condition selected is UNCONDITIONAL, a branch will always occur when MCI6 negates. If one of the four input signals is selected, MC BRANCH will assert only if that signal is *not* true. The branch condition selected will remain until another BRS instruction places a new select code into the branch condition register.

The PAGE NO./START VECTOR instruction causes one of two different actions, depending on the state of bit MCI4 of the instruction word. If MCI4 is false, it is a PAGE NO. instruction only which latches up MCI2 and MCI3 into the page number multiplexer as MC P6 and MC P7. MC P6 and MC P7 are the two most significant bits of the address input to the program counter. During a branch instruction, they select the page* to which the program will branch. If MCI4 is true, the instruction is a START VECTOR and PAGE NO. instruction. The next transition of MC CLOCK sets the START VECTOR flip-flop, asserting MC VECTOR XCT. The assertion of MC VECTOR XCT inhibits the control ROM and enables the start ROM as described earlier in this section. The page number multiplexer gets latched up just as in a PAGE NO. instruction except that the true state of MCI4 selects the FMT0 and FMT1 inputs as the MC P6 and MC P7 outputs for the program counter.

4.2.11.8 Program Errors – In addition to checking for data parity errors (Paragraph 4.2.11.6), the bit fiddler also checks for parity errors in the program instruction words, and for illegal formats and improper commands that may be input to the TM03.

Each program instruction is checked for odd parity in the MCI parity checker. Bit MCI7 of each word is the parity bit. If a parity error is detected, MC ERROR asserts, inhibiting the MC CLOCK signal and thereby stopping the program. The instruction word checked by the MCI parity checker is the one just executed. Thus when a program halt occurs, the instruction preceding the one now being output from the control ROM is the faulty one. The assertion of MC ERROR also sets the board fault flip-flop. The flip-flop illuminates the BOARD FAULT light and asserts MC BF FMTE to the error register in the MBI module.

Drawing M8915-8 lists all the address locations for the start vector ROM. Only six of these are legal addresses. The others result from illegal format coding or improper commands, such as write reverse. The SET/CLR decoder is utilized to sense illegal addressing of the start ROM. Note that each illegal instruction word contains a SET/CLR instruction (MCI0, 1, 6) and a MCI2, 3, 4 code of 6_8 which asserts the SET FMTE output of the decoder. However, only two of the four format bits are applied to the start ROM. The remaining two (FMT0, FMT1) are checked by an illegal format detector. The detector monitors all four format bits and output MC INST FMT ERR (instruction format error) when an illegal combination is sensed. Only four format codes are legal and these are shown in Table 4-7.

Table 4-7 Legal Format Codes

FMT 3	FMT 2	FMT 1	FMT 0	Mode
0	0	0	0	PDP-10 Core Dump
0	0	1	1	PDP-10 Compatible
1	1	0	0	PDP-11 Normal
1	1	1	0	PDP-15 Normal

Neither SET FMTE nor MC INST FMT ERR asserts MC BOARD FAULT or illuminates the BOARD FAULT light; however they do assert MC BF FMTE to the error register in the MBI module.

*Refer to drawing M8915-9, -10, and to Paragraph 4.2.11.10.

4.2.11.9 Program Timing – Program timing and synchronization are obtained by a crystal oscillator generating a 15.6* MHz MC CLOCK signal. The microcontroller ROM specifies an instruction, sets up the instruction parameters, and executes the instruction, all under timing control of MC CLOCK. For purposes of this discussion, the leading and trailing edges of MC CLOCK are defined as its assertion and negation, respectively. The program operations timed to the leading and trailing edge of MC CLOCK are as follows:

Leading Edge

1. Latch and execute selected instruction in accordance with instruction parameters. This means one of the following:

   a. Transfer a data nibble or zero-fill a latch.
   b. Assert one of the six SET/CLR commands.
   c. Establish a new branch condition.
   d. Change page number bits P6 and P7.

2. Increment the PC counter or load the PC counter with a branch address if BRANCH is true.

Trailing Edge

1. Control ROM fetches the instruction word addressed by MC A0 – MC A7.

2. Check parity of instruction word which was just executed.

3. Assert MC BRANCH if instruction is a branch instruction and if branch conditions are met.

4. Cause start ROM to branch to operational routine if instruction is a START VECTOR and PAGE NO. instruction.

4.2.11.10 Operational Flow Diagrams – Sheets M8915-9 and -10 show a program listing of the microcontroller ROM. MC ENAB SYNC is the MSB of the control ROM address. With MC ENAB SYNC false, the program addresses are confined to sheet 9 (addresses 000_8 to 377_8). When MC ENAB SYNC is true, the program addresses are on sheet 10 (addresses 400_8 to 777_8). The second and third most significant bits of the control ROM address (MC A7, MC A6) are established by the two page number bits, MC P7 and MC P6. The page number bits locate four pages of instructions when MC ENAB SYNC is true and another four pages when MC ENAB SYNC is false. Address bits MC A5 – MC A0 locate the individual instructions within each page. The flow diagrams in this section illustrate the routines listed on sheets M8915-9, -10. The diagrams contain key address locations to establish a correlation between them and the program listings.

The program startup flow diagram illustrates the startup sequence and the selection of the specific routine to be performed. The other diagrams show the sequence of events in each of the 12 routines. The flow diagrams do not involve any functions or operations not already described in preceding paragraphs. They serve to tie the steps of an operation together as they occur during program execution.

*M8915-YA only. The M8915 bit fiddler uses a 10.0 MHz crystal oscillator which cannot be used with 317.5 cm/s (125 in/s) transports (TU77).

Program Startup (Figure 4-49) – The assertion of MAS CLR initializes the M8915-YA module and sets the program counter to zero. The assertion of MC SET RIGHT occurs during initialize. (This is essential if the program selects a PDP-11 read operation or a PDP-15 read operation, because these routines do not contain a SET RIGHT instruction.) Next the program enters the idle mode where latches A through E are zero-filled. The program then waits for the assertion of BF ENABLE and AEMD. When this occurs the program jumps to the GO routine and waits for AEMD to negate. After the negation of AEMD, MC VECTOR XCT asserts, enabling the start vector ROM which branches the program to the address of 1 of the 12 operational routines.

PDP-11 Write Forward (11-NORMAL) (Figure 4-50) – The PDP-11 write forward (11-NORMAL) routine starts at location 421_8. The program asserts MC SET RIGHT to select the PDP-11 format for the 16-bit input word. MC SET SCLK asserts to request that input data be placed on the Massbus. When WCLK is received, the 16-bit input word is clocked into the multiplexer and into latches A through D. The program then transfers latch C to F and latch D to G. The 8-bit byte, now in latches F and G, and a parity bit are transmitted to the TCCM or the tape control NRZI module as a tape frame character. The program waits for the assertion of WRT STRB to signify that the TM03 write logic is ready for the next character. When WRT STRB asserts, and if BF ENABLE is still true, the data nibbles in latches A and B are transferred to latches F and G, respectively, and another tape frame character, along with its parity bit, are available to the output write logic. When the next WRT STRB is received, BF ENABLE is checked and if still true, the cycle is repeated for the next data word received from the Massbus.

If BF ENABLE is found to be false when checked by the program, MC ENAB SYNC is negated, which returns the program to the idle mode.

PDP-11 Write Forward (15-NORMAL) (Figure 4-51) – The PDP-11 write forward (15-NORMAL) routine starts at location 621_8. The instruction routine is identical to the PDP-11 write forward routine except that latches A and B (bits 15–08) are used for the first tape character and latches C and D (bits 07–00) are used for the second character. (See Paragraph 4.2.11.2 for a discussion of the various data transfer formats.)

PDP-11 Read Forward Normal/PDP-11 Read Reverse (15-NORMAL) (Figure 4-52) – The PDP-11 read forward normal and the PDP-11 read reverse (15-NORMAL) routines are identical. The PDP-11 read forward routine starts at location 417_8. The PDP-11 read reverse (15-NORMAL) routine starts at location 605_8. The assertion of RDS clocks a tape character into latches F and G. If BF ENABLE is true, the program transfers latch F to C and latch G to D. The program then waits for the next RDS pulse which clocks the next tape character into F and G. If BF ENABLE is still true, the data nibbles in latches F and G are transferred to latches A and B, respectively. Latches A through D then transfer their contents to the output multiplexer, which is still in the SET RIGHT format from the initialize routine. MC SET SCLK asserts and transmits the multiplexer output (D15 TM – D00 TM) to the Massbus along with the parity bit.

If, during a check of the state of BF ENABLE, it is found to be false, MC ENAB SYNC is negated and the program returns to the idle mode. If BF ENABLE goes false after a tape character has been clocked into latches C and D, the other two latches (A and B) are zero-filled and MC SET SCLK is asserted before the program returns to idle. Thus all data read from tape is placed on the Massbus regardless of when the data transfer is terminated.

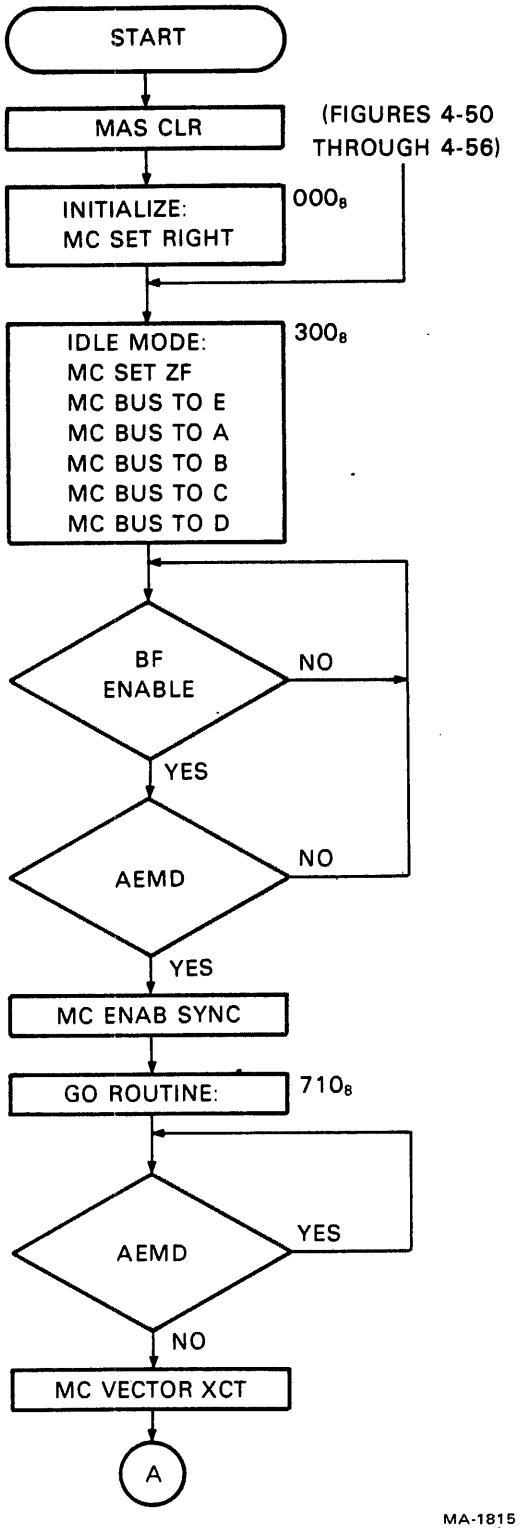


Figure 4-49 Program Startup Flow Diagram (Sheet 1 of 2)

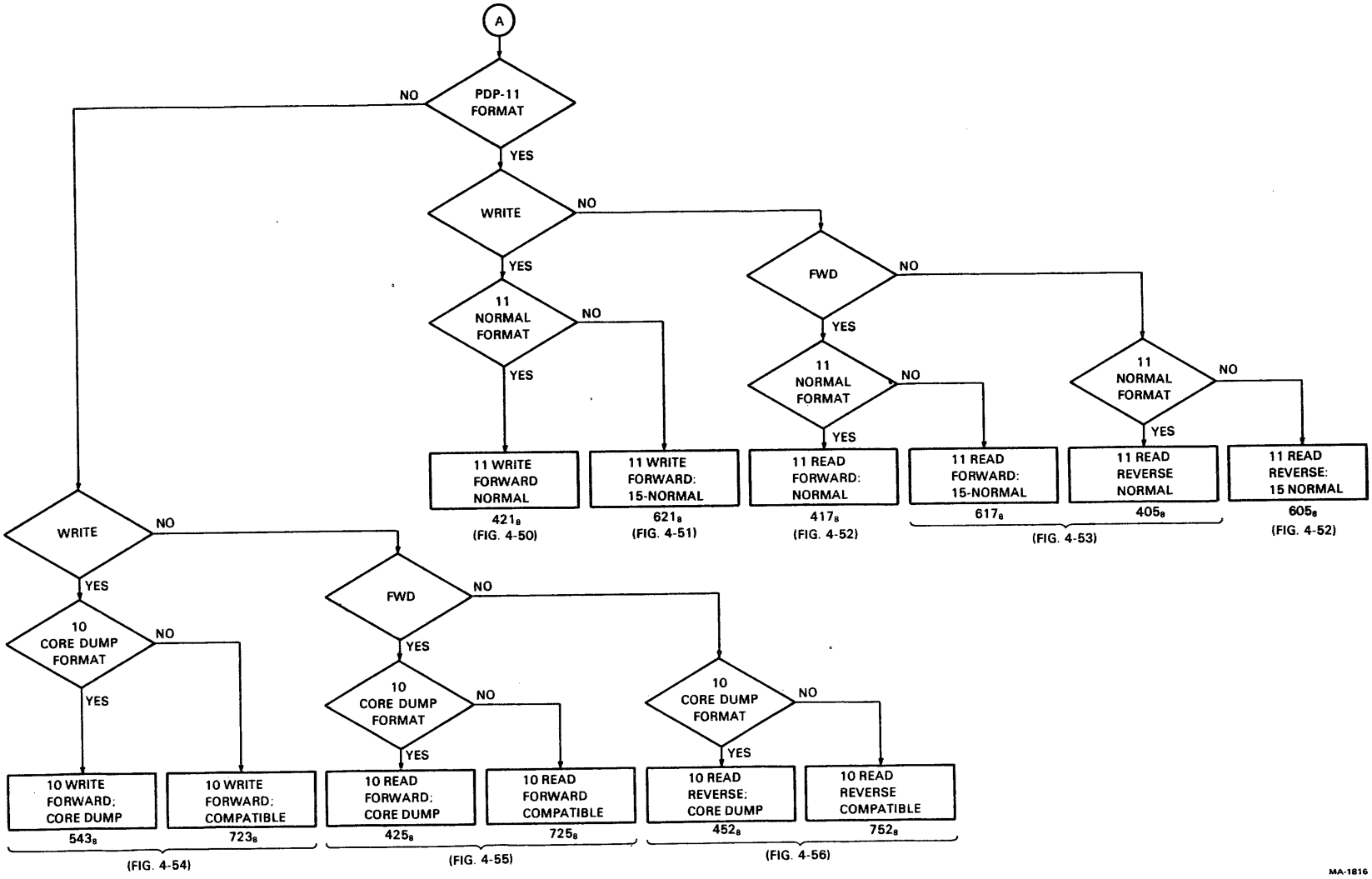


Figure 4-49 Program Startup Flow Diagram (Sheet 2 of 2)

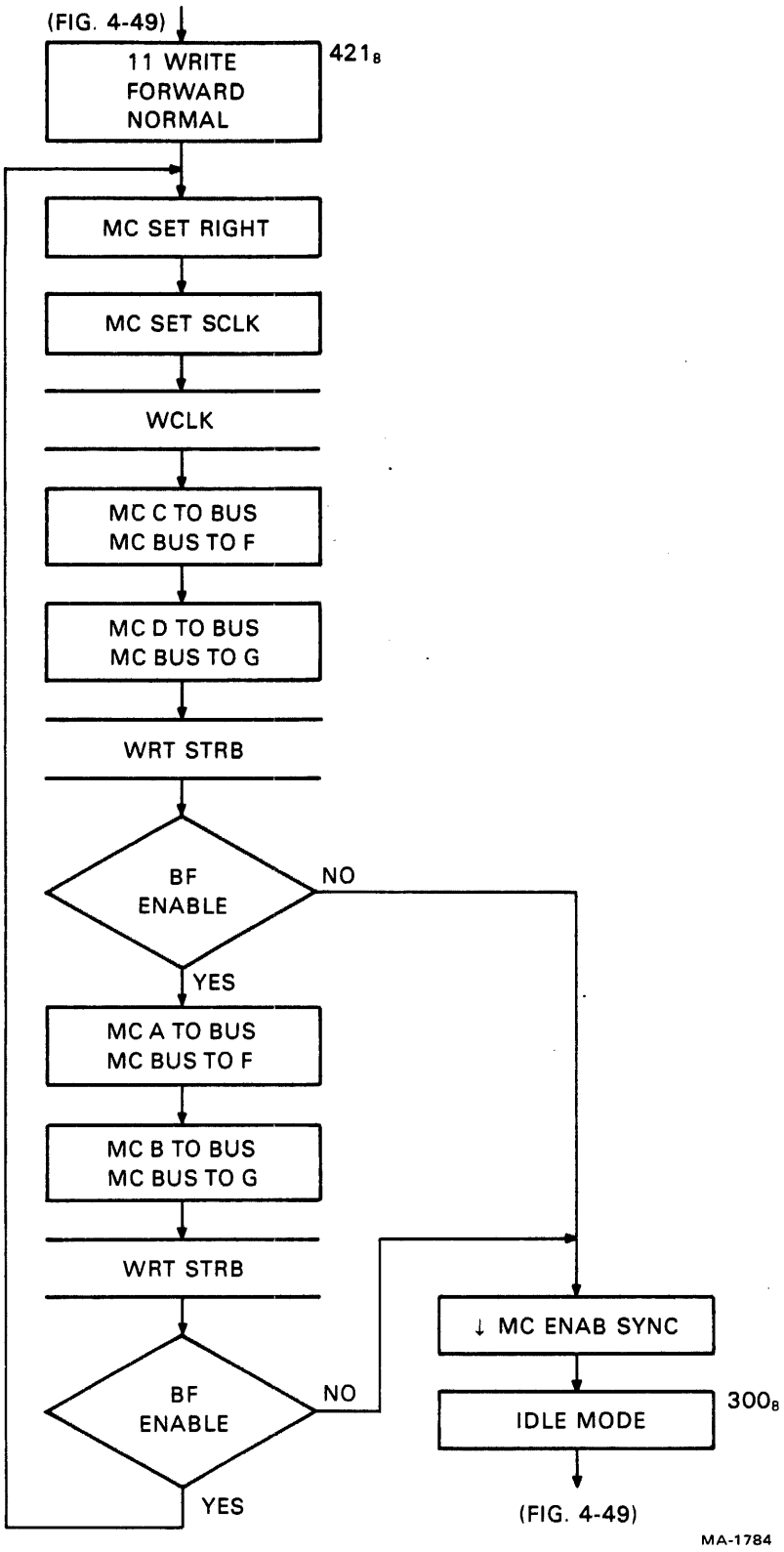


Figure 4-50 PDP-11 Write Forward Normal Flow Diagram

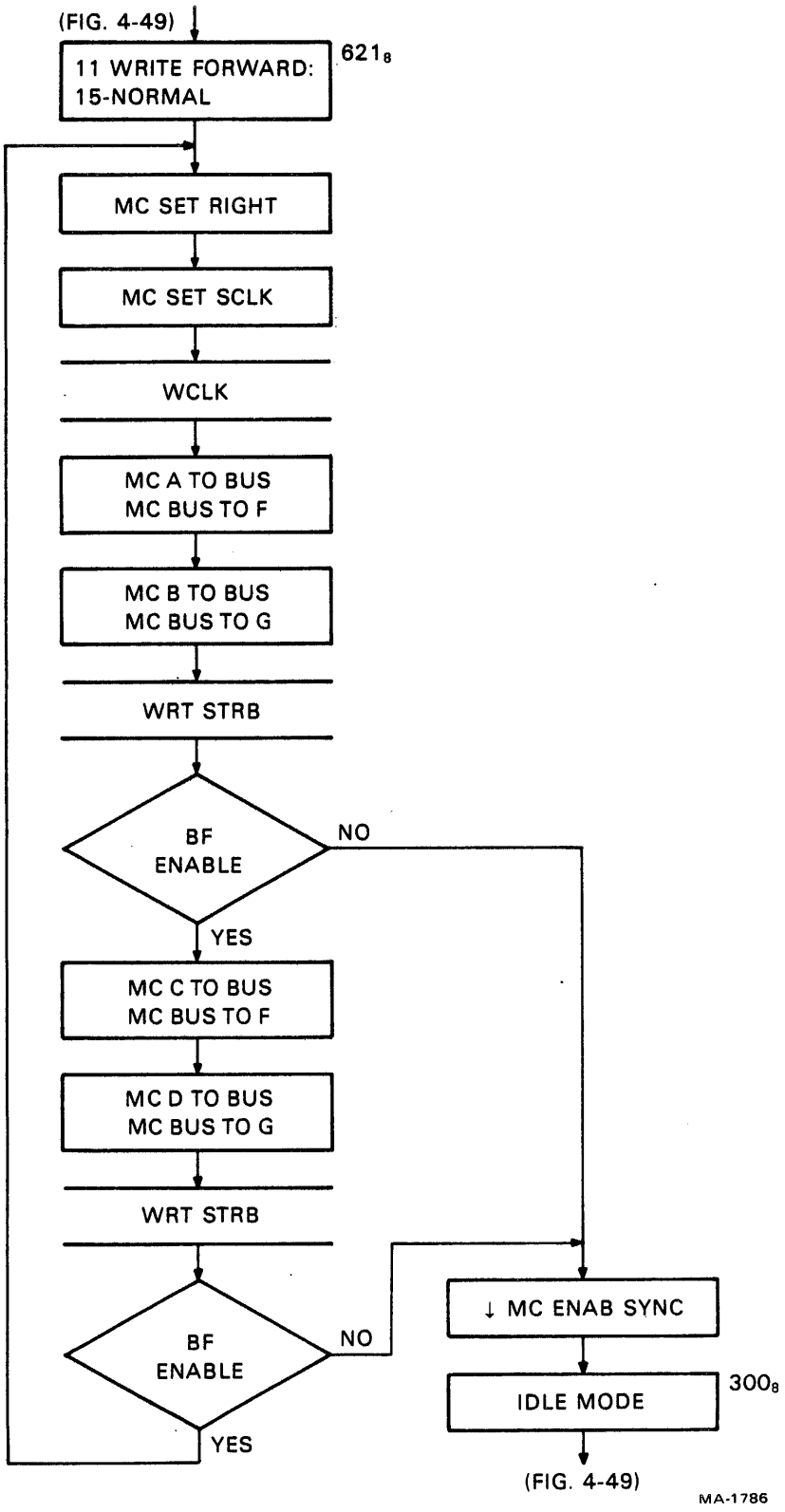


Figure 4-51 PDP-11 Write Forward: (15-Normal) Flow Diagram

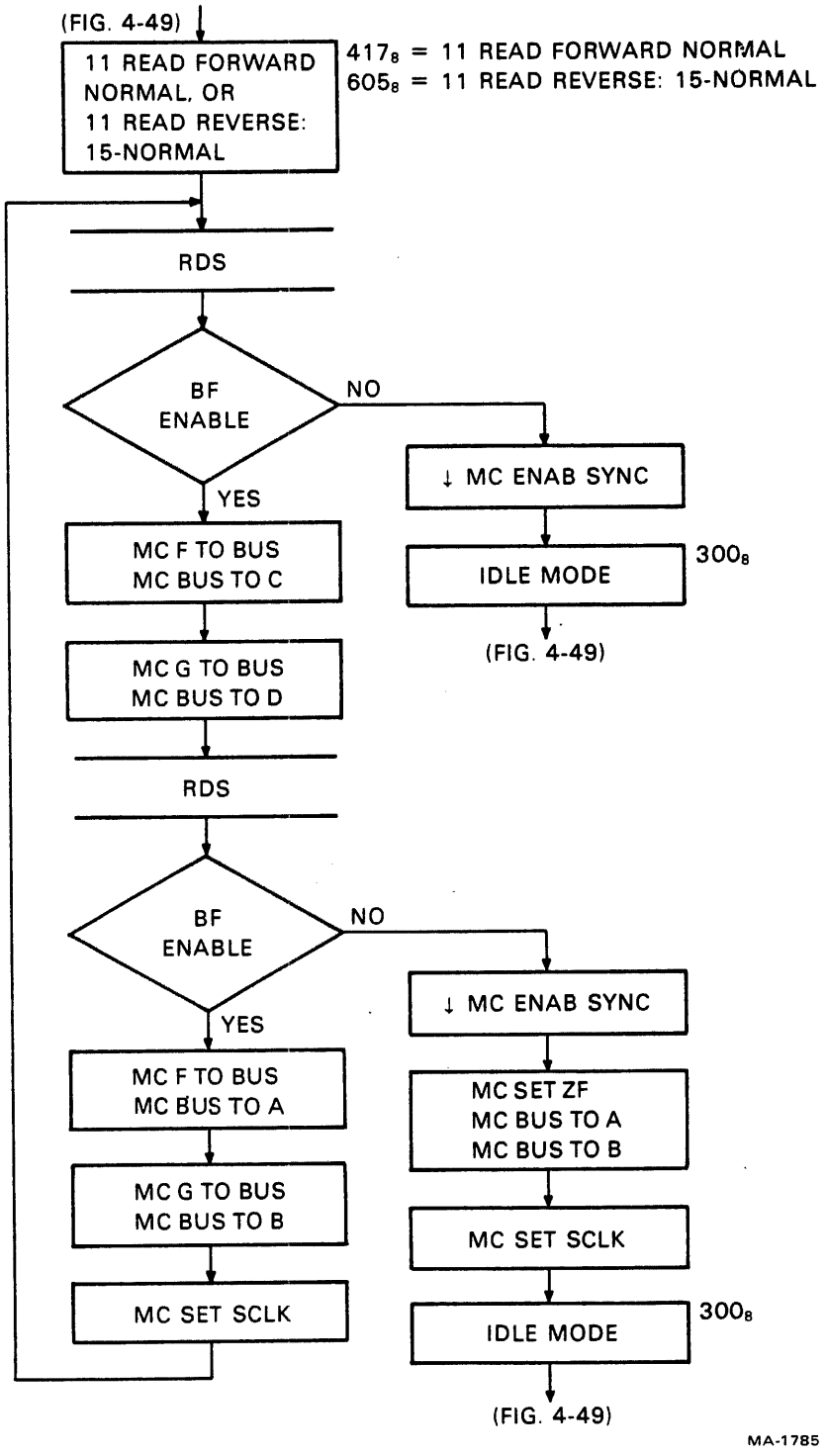


Figure 4-52 PDP-11 Read Forward Normal/PDP-11 Read Reverse (15-Normal) Flow Diagram

PDP-11 Read Reverse Normal/PDP-11 Read Forward (15-NORMAL) (Figure 4-53) – The PDP-11 read reverse normal and the PDP-11 read forward (15-NORMAL) routines are identical. The PDP-11 read reverse normal routine starts at location 405_8. The PDP-11 read forward (15-NORMAL) routine starts at location 617_8. The assertion of RDS clocks a tape character into latches F and G. If BF ENABLE is true, the program transfers latch F to A and latch G to B. The program waits for the next RDS pulse, which clocks the next tape character into F and G. Then, if BF ENABLE is still true, the data nibbles in latches F and G are transferred to latches C and D, respectively. Latches A through D then transfer their contents to the output multiplexer, which is still in the SET RIGHT format from the initialize routine. MC SET SCLK asserts and transmits the multiplexer output (D15 TM – D00 TM) to the Massbus along with the parity bit.

If, during a check of the state of BF ENABLE, it is found to be false, MC ENAB SYNC is negated and the program returns to the idle mode. If BF ENABLE goes false with a tape character already clocked into latches A and B, the other two latches (C and D) are zero-filled and MC SET SCLK is asserted before the program returns to idle. Thus all data read from tape is placed on the Massbus regardless of when the data transfer is terminated.

PDP-10 Write Forward (Figure 4-54) – The PDP-10 write forward operation is executed in the compatible or core dump mode. In the compatible mode, a 36-bit PDP-10 word is written onto tape in four 8-bit bytes and the last four bits of the word are discarded. In the core dump mode, the entire 36-bit word is written onto tape in five 8-bit bytes with the last byte composed of 4 data bits and a 4-bit zero-fill. Figure 4-54 is a flow diagram of the PDP-10 write forward routines. Most of the diagram is common to both compatible and core dump operation. The portion of the diagram enclosed in dotted lines is only for PDP-10 compatible operation. Replacing this portion with the core dump portion converts the diagram into a PDP-10 core dump flow diagram.

The PDP-10 compatible routine starts at location 723_8. The PDP-10 core dump routine starts at location 543_8. The program asserts the SET LEFT format and then MC SET SCLK to request data input on the Massbus. When WCLK is received, the 18-bit data input is clocked into the input multiplexer and into latches A through D and latch E left. (WCLK asserts DR GET LEFT, which clocks two bits into latch E left.) The program then transfers latch A to F and latch B to G. The 8-bit byte is now in latches F and G, along with a parity bit, are transmitted to the TCCM or the tape control NRZI module as a tape frame character. The program waits for the assertion of WRT STRB to signify that the TM03 write logic is ready for the next character. When WRT STRB asserts, and if BF ENABLE is still true, the data nibbles in latches C and D are transferred to latches F and G, respectively, and another tape frame character, along with its parity bit, are available to the output write logic. When the next WRT STRB is received, BF ENABLE is checked and if still true, the SET RIGHT format is asserted and MC SET SCLK is issued to request the second half of the input word. When WCLK is received, the 18-bit data input is clocked into the input multiplexer and into latches A through D and latch E right. (WCLK asserts DR GET RIGHT which clocks two bits into latch E right.) The program then transfers latch E (now loaded with four bits) to F and latch A to G. The 8-bit byte now in latches F and G, along with a parity bit, are transmitted to the output write logic as the third tape frame character. When the next WRT STRB is received, BF ENABLE is checked and if still true, latches B and C are transferred to latches F and G, respectively, forming the fourth tape character. When the fourth tape character has been transmitted from F and G and the next WRT STRB is received, another check is made of BF ENABLE.

If BF ENABLE is still true and the operating mode is PDP-10 compatible, the program returns to location 723_8 to prepare for the next 18-bit data input. The 4-bit nibble still in latch D is not transferred to tape.

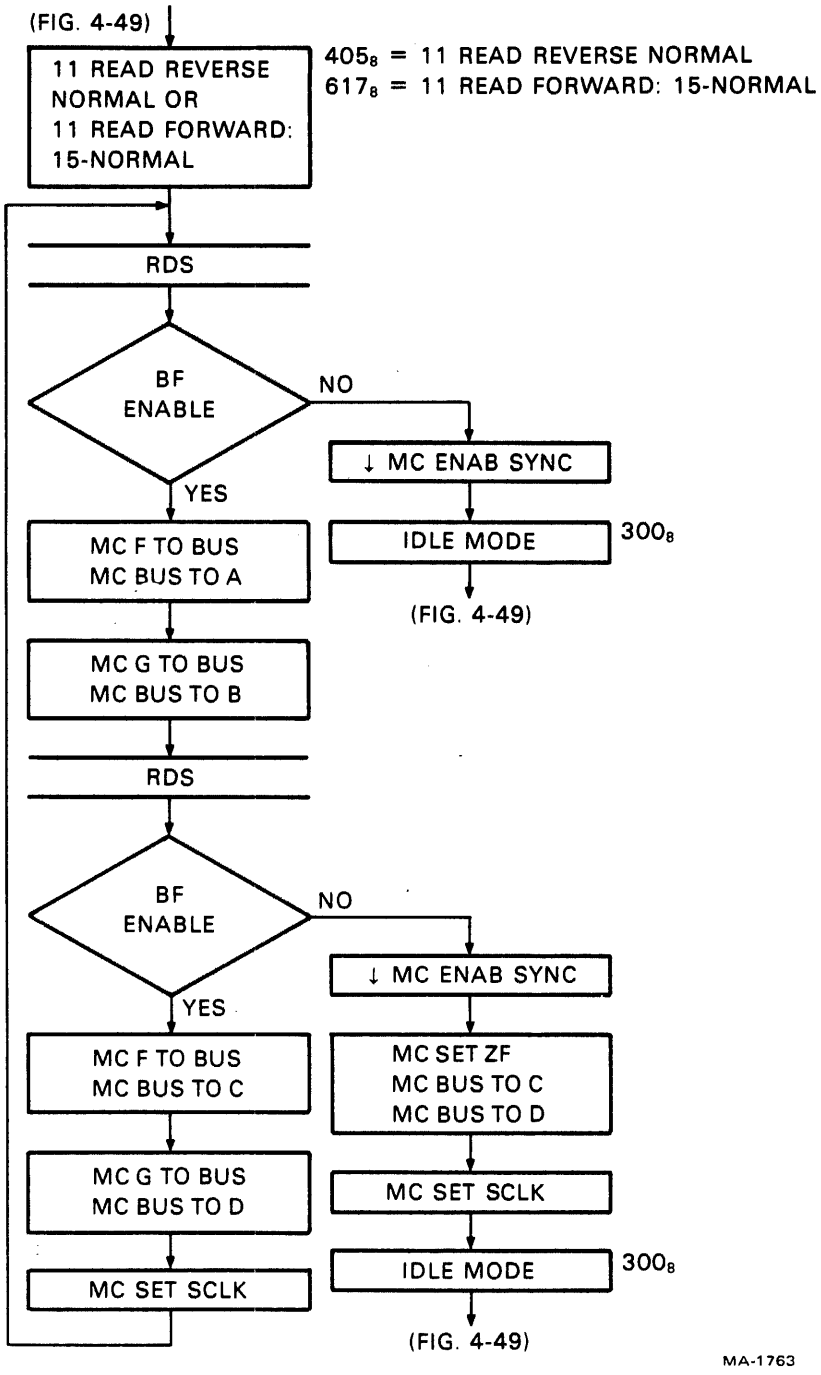


Figure 4-53 PDP-11 Read Reverse Normal/PDP-11 Read Forward (15-Normal) Flow Diagram

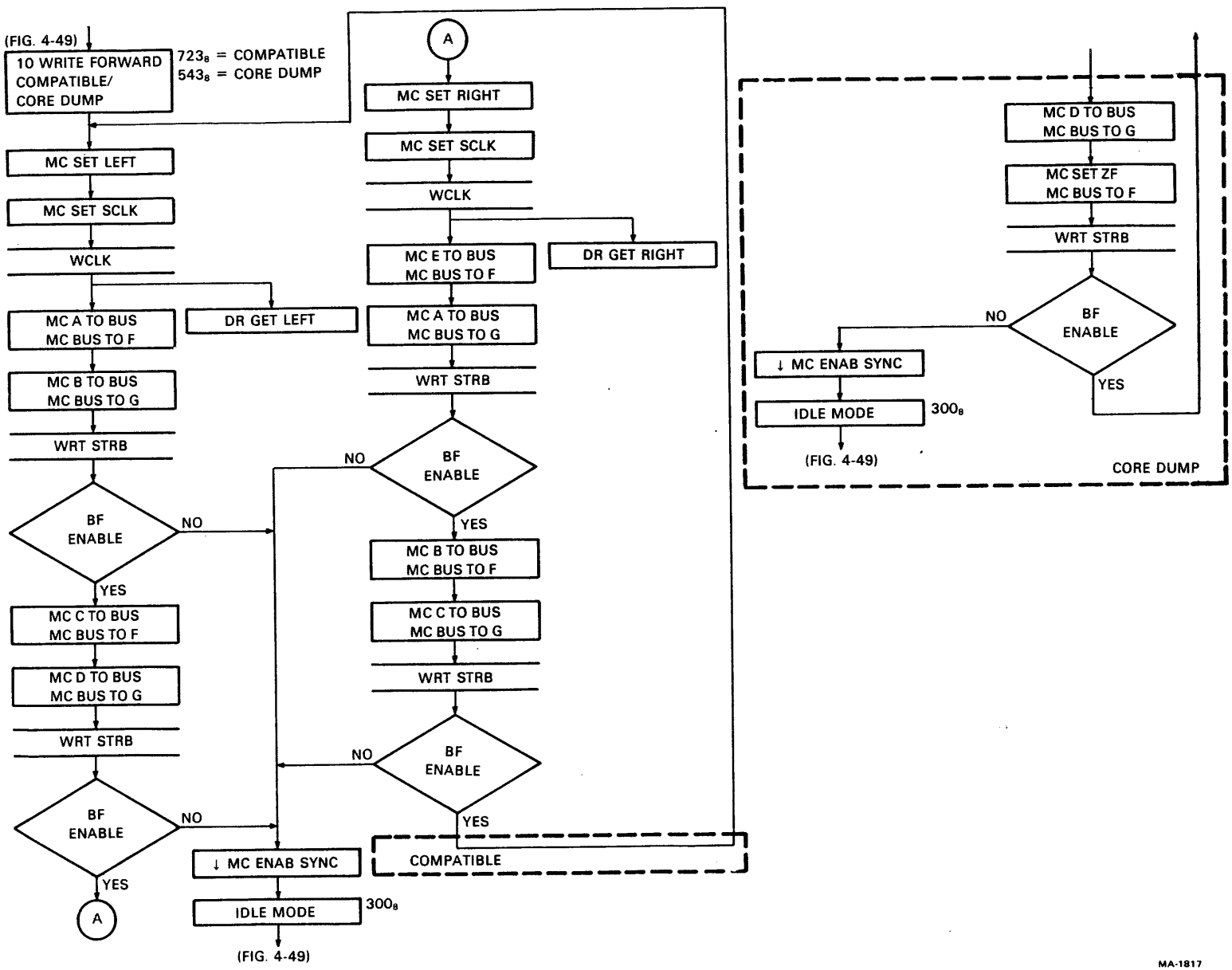


Figure 4-54 PDP-10 Write Forward Flow Diagram

If BF ENABLE is still true and the operating mode is PDP-10 core dump, the program continues and transfers the nibble in latch D to latch G and then does a zero-fill into latch F. The output write logic takes the data in latches F and G for the fifth tape character and then asserts WRT STRB. If BF ENABLE is still true, the program returns to location 543_8 to prepare for the next 18-bit data input.

If BF ENABLE checked false at any point in the PDP-10 write routines, MC ENAB SYNC is negated and the program returns to the idle mode.

PDP-10 Read Forward (Figure 4-55) – The PDP-10 read forward operation is executed in the compatibility or core dump mode. In the compatibility mode, four 8-bit characters (32 bits total) are read from tape and placed onto the Massbus as 18 bits of one data transfer and 14 bits of a second data transfer. The remaining four bits of the second data transfer are zero-filled. In the core dump mode, five 8-bit characters (40 bits total) are read from tape and placed onto the Massbus as two 18-bit data transfers. The fifth tape character contains a 4-bit zero-fill which is discarded. Figure 4-55 is a flow diagram of the PDP-10 read forward routines. Most of the diagram is common to both compatible and core dump operation. The portion of the diagram enclosed in dashed lines is only for PDP-10 compatible operation. Replacing this portion with the core dump portion converts the diagram into a PDP-10 core dump flow diagram.

The PDP-10 compatible routine starts at location 725_8. The PDP-10 core dump routine starts at location 425_8. The assertion of RDS clocks a tape character into latches F and G. If BF ENABLE is true, the program transfers latch F to A and latch G to B. When RDS clocks the second tape character into latches F and G, BF ENABLE is again checked. If found to be still true, the program transfers the data nibbles in latches F and G to latches C and D, respectively. When RDS clocks the third tape character into latches F and G, BF ENABLE is again checked. If found to be still true, the program transfers the nibble in latch F to latch E and then asserts the SET LEFT format. MC SET SCLK then asserts and clocks the data from latches A through E (only two bits from latch E) to the Massbus via the output multiplexer. The program then transfers the nibble in latch G to latch A. The next RDS pulse clocks the fourth tape character into latches F and G. If BF ENABLE is still true, latches F and G are transferred to B and C, respectively.

If the operating mode is PDP-10 compatible, the program will zero-fill latch D, assert a SET RIGHT format to the output multiplexer, and assert MC SET SCLK. The assertion of MC SET SCLK clocks the data from latches A through E (only two bits from latch E) to the Massbus via the multiplexer. The program then returns to location 725_8 and the cycle is repeated.

If the operating mode is PDP-10 core dump, the program waits for RDS to assert and clock the fifth tape character into latches F and G. If BF ENABLE is still true, the nibble in latch G is transferred to latch D (latch F is discarded). The program then asserts the SET RIGHT format to the output multiplexer and asserts MC SET SCLK. The assertion of MC SET SCLK clocks the data from latches A through E (only two bits from latch E) to the Massbus via the multiplexer. The program then returns to location 425_8 and the cycle is repeated.

If BF ENABLE checked false at any point in the PDP-10 read forward routines, MC ENAB SYNC is negated and the program returns to the idle mode. If tape data has already been transferred to some of the A through E latches, the remaining latches are zero-filled, a format state is asserted (SET LEFT or SET RIGHT), and MC SET SCLK is asserted before the program returns to idle. Thus all data read from tape is placed on the Massbus regardless of when the data transfer is terminated.

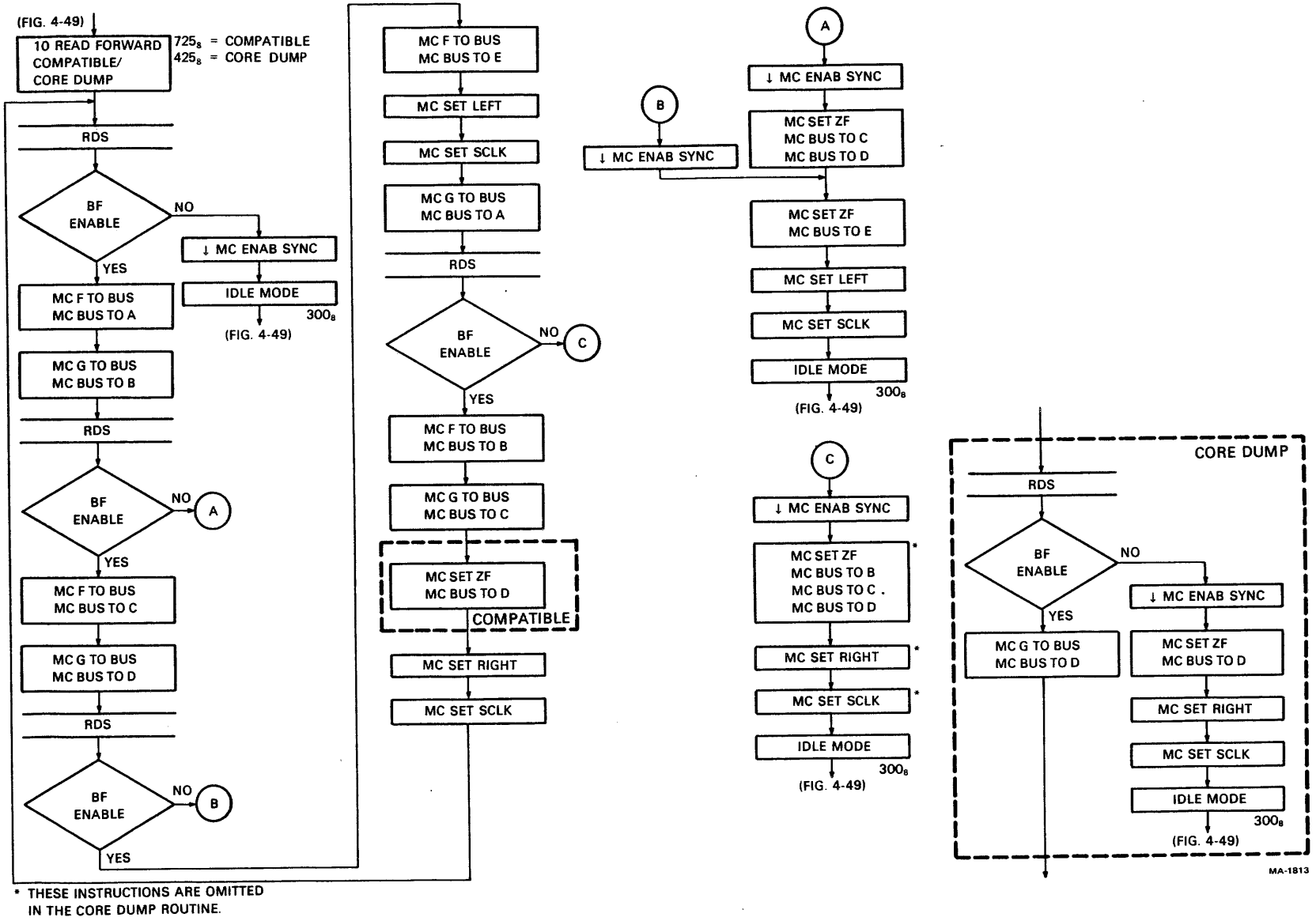


Figure 4-55 PDP-10 Read Forward Flow Diagram

PDP-10 Read Reverse (Figure 4-56) - A PDP-10 read reverse operation reads data from tape in the reverse sequence from which it was written. The PDP-10 read reverse operation is executed in the compatibility or core dump mode. In the compatibility mode, four 8-bit characters (32 bits total) are read from tape and placed onto the Massbus as 14 bits of one data transfer (plus a 4-bit zero-fill) and 18 bits of a second data transfer. In the core dump mode, five 8-bit characters (40 bits total) are read from tape and placed onto the Massbus as two 18-bit data transfers. (The first tape character read contains a 4-bit zero-fill which is discarded.) Figure 4-56 is a flow diagram of the PDP-10 read reverse routines. Most of the diagram is common to both compatible and core dump operation. The portion of the diagram enclosed in dashed lines is only for PDP-10 compatible operation. Replacing this portion with the core dump portion converts the diagram into a PDP-10 core dump flow diagram.

The PDP-10 compatible routine starts at location 752_8. The routine looks for the assertion of RDS, which clocks a tape character into latches F and G. If BF ENABLE is true, the program zero-fills latch D as only 14 of the 18 bits of the first Massbus transfer will be data bits.

The PDP-10 core dump routine starts at location 452_8. The routine looks for the assertion of RDS, which clocks a tape character into latches F and G. If BF ENABLE is true, the program transfers latch G to latch D. The 4-bit nibble in latch F is a zero-fill and is ignored. When RDS clocks the second tape character into latches F and G, BF ENABLE is again checked. If found to be true, the program will continue.

Continuation of the PDP-10 read reverse routine is identical for both the compatible and core dump modes. The program transfers latch F to B and latch G to C. When RDS clocks the next tape character (the second character for compatible operation or the third character for core dump) into latches F and G, BF ENABLE is again checked. If found to be still true, the program transfers the data nibbles in latches F and G to latches E and A, respectively. The program then asserts the SET RIGHT format followed by MC SET SCLK, which clocks the data from latches A through E (only two bits from latch E) to the Massbus via the output multiplexer. RDS then clocks the next tape character into latches F and G. If BF ENABLE is still true, latches F and G are transferred to C and D, respectively. The next RDS pulse clocks the last tape character (of this PDP-10 word) into latches F and G. If BF ENABLE is still true, the data nibbles in latches F and G are transferred to A and B, respectively. The program then asserts the SET LEFT format, followed by MC SET SCLK, which clocks the data from latches A through E (only two bits from latch E) to the Massbus via the multiplexer. The program then returns to location 752_8 if the mode is compatible, or to location 452_8 if the mode is core dump, and the cycle is repeated.

If BF ENABLE checked false at any point in the PDP-10 read reverse routines, MC ENAB SYNC is negated and the program returns to the idle mode. If tape data has already been transferred to some of the A through E latches, the remaining latches are zero-filled, a format state is asserted (SET LEFT or SET RIGHT), and MC SET SCLK is asserted before the program returns to idle. Thus all data read from tape is placed on the Massbus, regardless of when the data transfer is terminated.

4.2.12 Bit Fiddler Read (M8906)

This paragraph discusses the operation of the M8906 bit fiddler during a read data operation (reference Figure 4-4). The M8906 bit fiddler is used in PDP-11 systems. PDP-10 systems utilize an M8915 bit fiddler which is described in Paragraph 4.2.11.

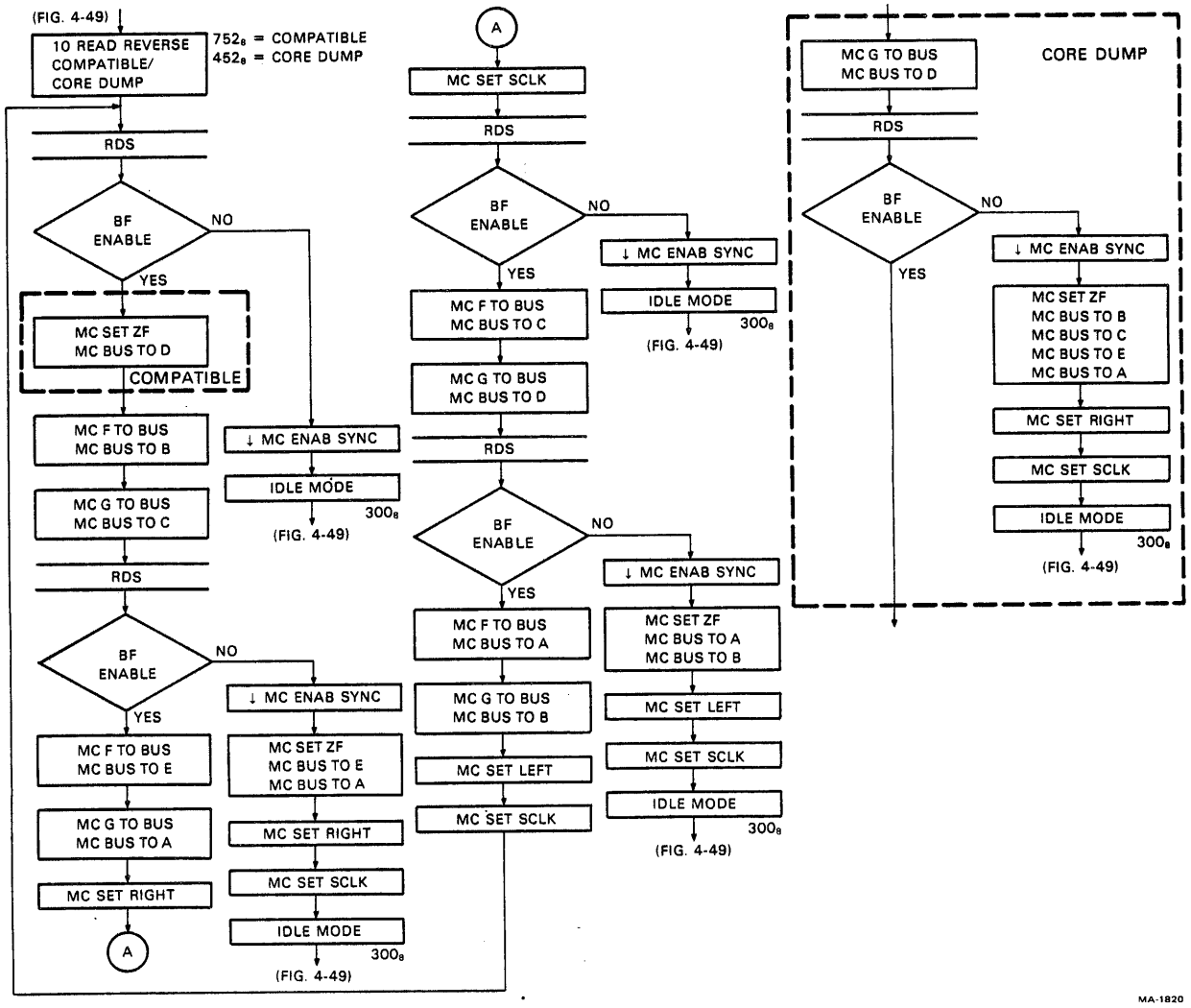


Figure 4-56 PDP-10 Read Reverse Flow Diagram

4.2.12.1 M8906 Bit Fiddler Operating Modes – When OCC is asserted on the Massbus, the bit fiddler is enabled (BF ENABLE H asserted on MBI9). [Reference the M8906 schematics and the M8906 bit fiddler read operation flowchart (Figure 4-57).] When DRIVE SET PLS is generated, tape motion is started and the bit fiddler is initialized by P BF RUN H (generated by the signal AEMD on BF2). The initial state of the bit fiddler during a read operation is determined by the tape data format and the direction of tape motion. These parameters determine the initial states of the select A and select B flip-flops. The format also determines the manner in which these flip-flops will be toggled (Table 4-8).

Table 4-8 Bit Fiddler Initialization/Operation

	Format Mode	Select A		Select B	
		Initial	Toggled by	Initial	Toggled by
Forward Tape Motion	Normal Mode	Clear	Toggling inhibited	Clear	RDS
	Core Dump	Clear	RDS	Clear	Alternate RDS
	PDP-15 Mode	Clear	Toggling inhibited	Set	RDS
Reverse* Tape Motion	Normal Mode	Clear	Toggling inhibited	Set	RDS
	Core Dump	Clear	RDS	Set	Alternate RDS
	PDP-15Mode	Clear	Toggling inhibited	Clear	RDS

*Only normal mode and PDP-15 mode provide proper reassembly in read reverse.

The format select bits (FMT 0–3) of the tape control register are decoded in the bit fiddler (BF3) as shown in Table 4-9.

Table 4-9 Read Formatting Codes

FMT (0–3)				
3	2	1	0	Mode
1	1	0	0	Normal Mode
1	1	0	1	Core Dump
1	1	1	0	PDP-15 Mode

Any other combination produces a bit fiddler format error (BFFMTE).

4.2.12.2 M8906 Bit Fiddler Read Operation – Tape characters received from the maintenance register are checked for parity before being applied to the bit fiddler read multiplexer. If a parity error is detected, SET VPAR is asserted, which in turn asserts the INC/VPE error bit in the error register.

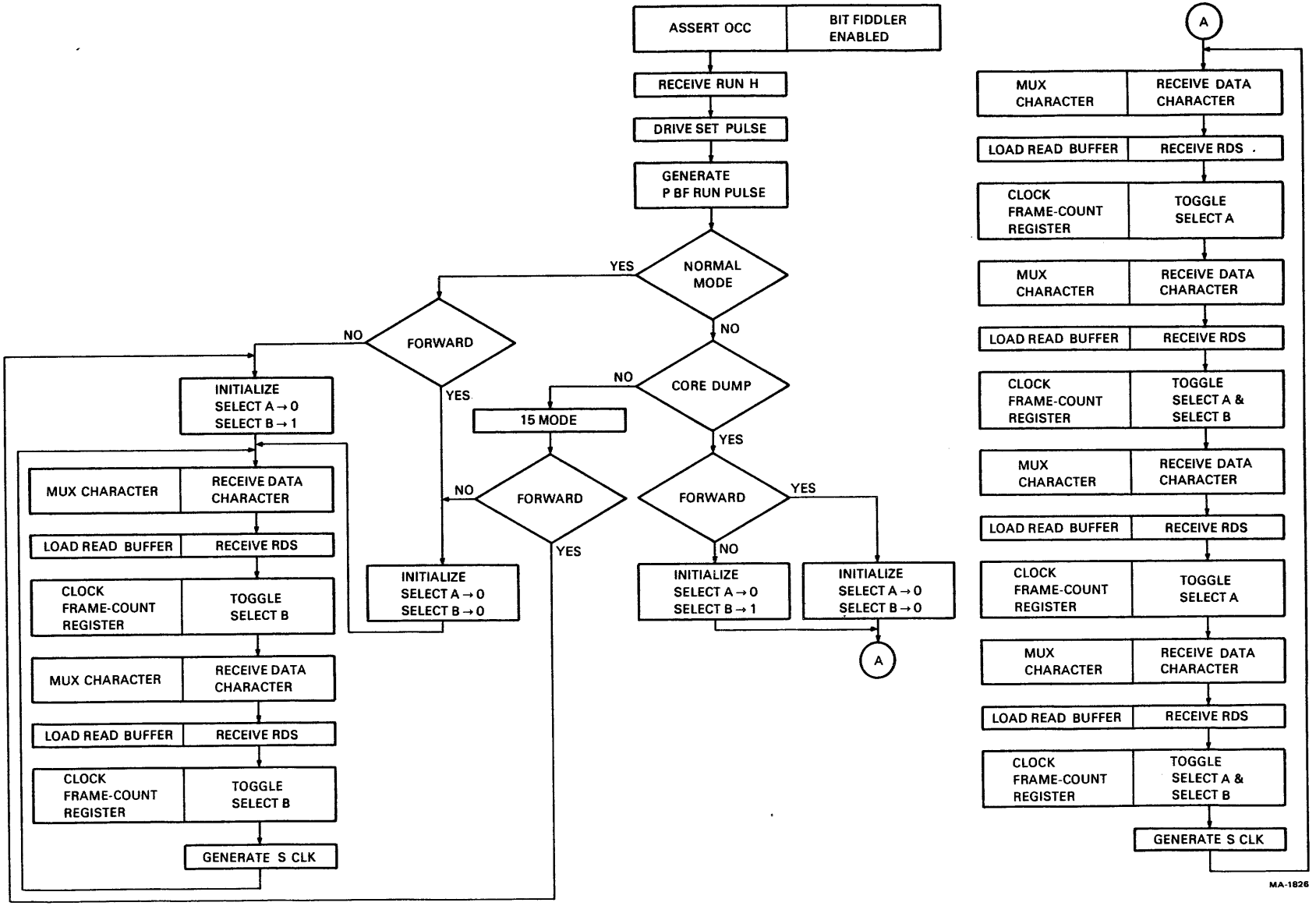


Figure 4-57 M8906 Bit Fiddler Read Operation Flowchart

When a tape data character becomes available on the read data C lines (RDC 0–7 on BF5), the bit fiddler receives RDS (BF2). This causes one or two of the read latches on BF5 to be loaded by CLK Ⓐ and/or CLK Ⓑ, or by CLK Ⓒ and/or CLK Ⓓ, depending on the states of SELECT A, SELECT B, and CORE DUMP. The states of SELECT B and/or SELECT A are now altered, and, when the next tape data character becomes available and RDS is received, one or two other read latches are loaded. The bit fiddler thus assembles 18-bit data words (bits 16 and 17 forced set) for transfer to the Massbus controller. Table 4-10 shows CLK Ⓐ, Ⓑ, Ⓒ, and Ⓓ sequences for the different formats and tape motion directions.

Table 4-10 CLK Ⓐ, Ⓑ, Ⓒ, and Ⓓ Sequences

Mode	Direction of Tape Motion	Sequence
Normal Mode	Foward	A&B→C&D→A&B→C&D→etc.
	Reverse*	C&D→A&B→C&D→A&B→etc.
Core Dump	Forward	A→B→C→D→A→B→C→D→etc.
	Reverse	C→D→A→B→C→D→A→etc.
15 Mode	Forward	C&D→A&B→C&D→A&B→etc.
	Reverse*	A&B→C&D→A&B→C&D→etc.

*Only normal mode and 15 mode provide proper reassembly in read reverse.

After each CLK Ⓐ, Ⓑ, Ⓒ, and Ⓓ cycle, an 18-bit data word, ready for transmission to the Massbus controller, is sitting on the data lines. The bit fiddler generates a parity bit, DPA TM, which will be transmitted with the data word.

When the data word is assembled, the Massbus transfer (MB XFR, BF2) flip-flop is clocked set. This produces a 1 μs pulse, SCLK, which is transmitted to the Massbus controller and causes it to strobe in the word on the data lines. SCLK also resets the MB XFR flip-flop. Consecutive tape data characters are assembled in the same manner, and each time a data word is ready, SCLK is generated to the Massbus controller.

Figure 4-58 is a timing diagram of bit fiddler operation in core dump mode during a read forward operation.

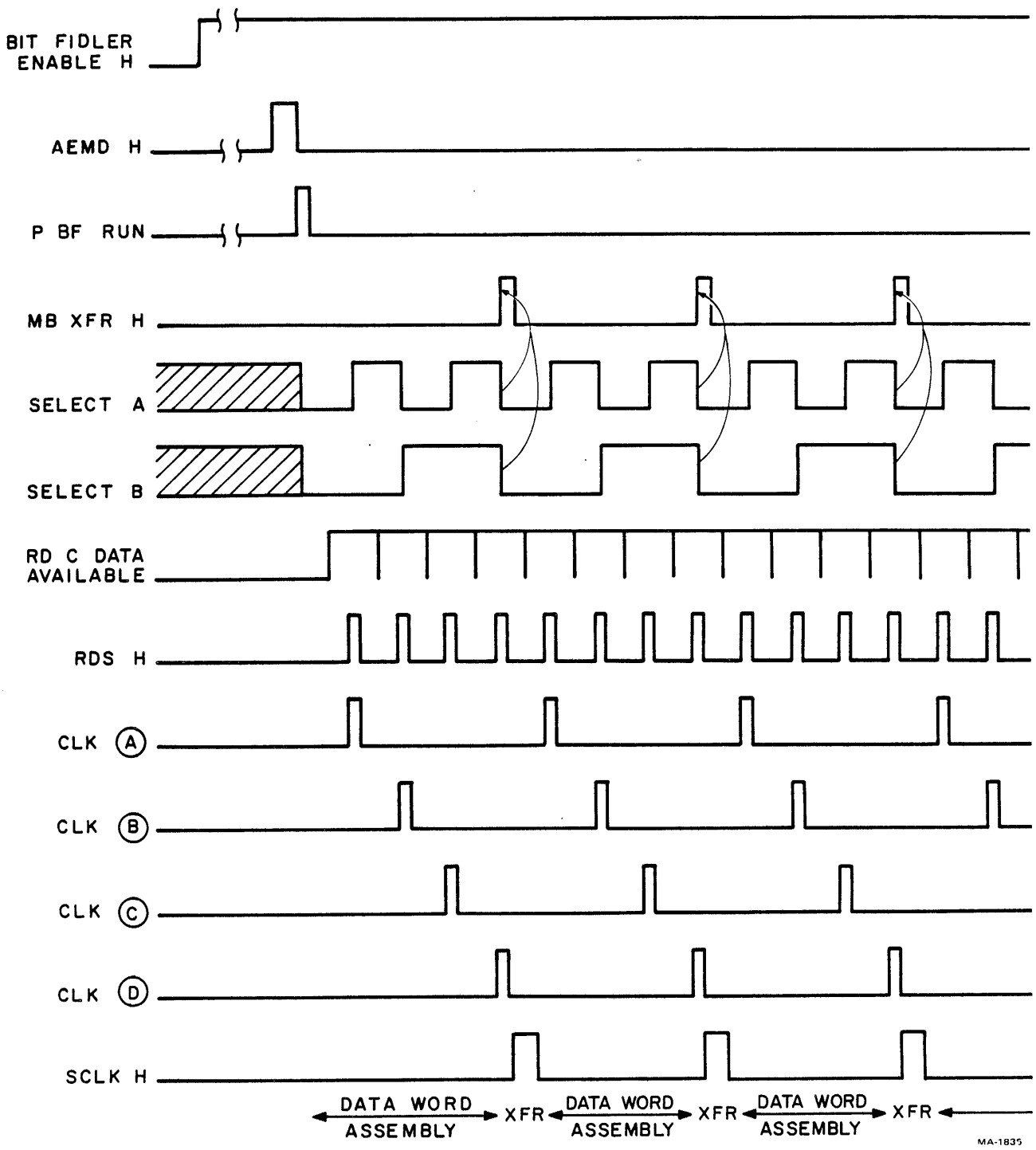


Figure 4-58 Bit Fiddler Read Forward Operation in Core Dump Mode

4.2.13 Bit Fiddler Write (M8906)

This paragraph discusses the operation of the M8906 bit fiddler during a write data operation (reference Figure 4-2). The M8906 bit fiddler is used in PDP-11 systems. PDP-10 systems utilize an M8915 bit fiddler, which is described in Paragraph 4.2.11.

4.2.13.1 Bit Fiddler Initialization – Reference the M8906 bit fiddler schematics and the bit fiddler write operation flowchart (Figure 4-59).

When the TM03 decodes a data transfer function code in the control register, OCC TM is asserted (MBI7); this enables the bit fiddler (BF ENABLE H, MBI9). When the Massbus controller is ready to transmit data, it places an 18-bit data word on the data lines of the data bus, places a parity bit associated with the data lines on the DPA line, and then asserts RUN H.

When the TM03 receives RUN H, DRV SET PLS is generated in the Massbus interface module (M8909-YA). DRV SET PLS produces AEMD H (TCCM3), a pulse which, on its trailing edge, triggers a one-shot (BF2) and generates P BF RUN H. P BF RUN H initializes the bit fiddler by setting or clearing the select A and select B flip-flops. Because WRITE L is asserted during a write data operation, P BF RUN H is gated and sets the MB XFR (Massbus transfer) flip-flop. MB XFR H produces a SCLK pulse, which resets the MB XFR flip-flop and is transmitted to the Massbus controller.

When the Massbus controller receives SCLK, it transmits WCLK to the TM03 and then places the next data word and its corresponding parity bit on the data bus. WCLK, enabled by BF ENABLE, produces CLK WRT BUF H, which loads the bit fiddler write buffer (BF4). Thus, in a data write operation, the first data word is transferred soon after, and as a consequence of, the assertion of RUN H. Subsequent data words are transferred only after the first data word has been converted to tape characters, i.e., after the motion delay is over (and in PE mode, after the preamble is written).

4.2.13.2 Bit Fiddler Formatting – The mode of bit fiddler operation during a data write is determined by the selected data format. The format select bits (FMT 0–3) of the tape control register are decoded in the bit fiddler as shown in Table 4-11.

Table 4-11 Write Formatting Codes

FMT (0–3)				
3	**2**	**1**	**0**	**Mode**
1	1	0	0	Normal Mode
1	1	0	1	Core Dump
1	1	1	0	PDP-15 Mode

Any other combination produces a bit fiddler format error (BFFMTE). The selected format determines the initial states of the select A and select B flip-flops, and also the manner in which the flip-flops are toggled (Table 4-12). SLCT A and SLCT B are multiplexed inputs (BF4) which determine the manner in which a data word stored in the write buffer is disassembled. Note that in core dump mode, WD BFO 4–7 are forced low. As SLCT A and/or SLCT B toggle, the data word is multiplexed into characters as indicated in Figure 4-60.

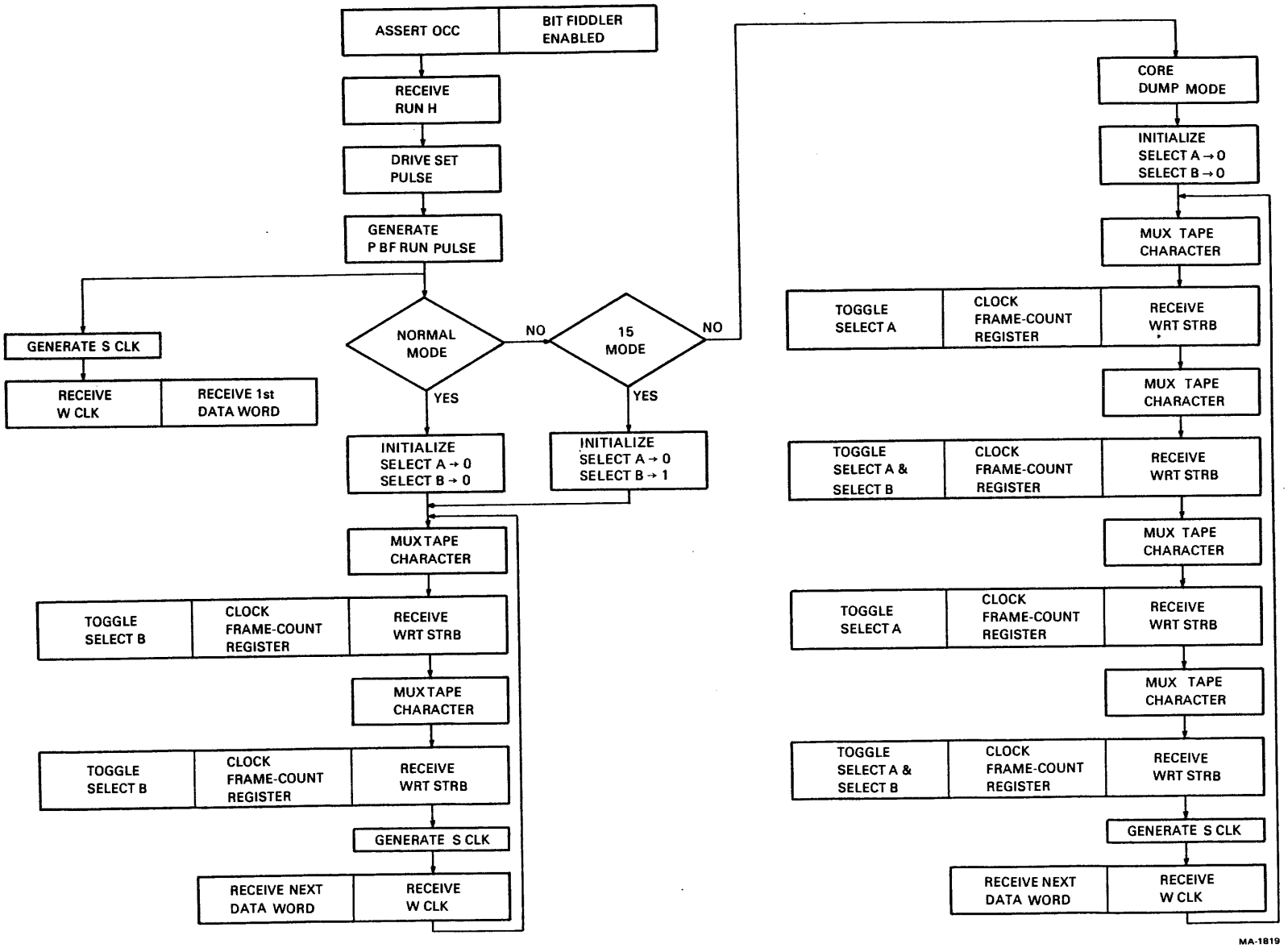


Figure 4-59 M8906 Bit Fiddler Write Operation Flowchart

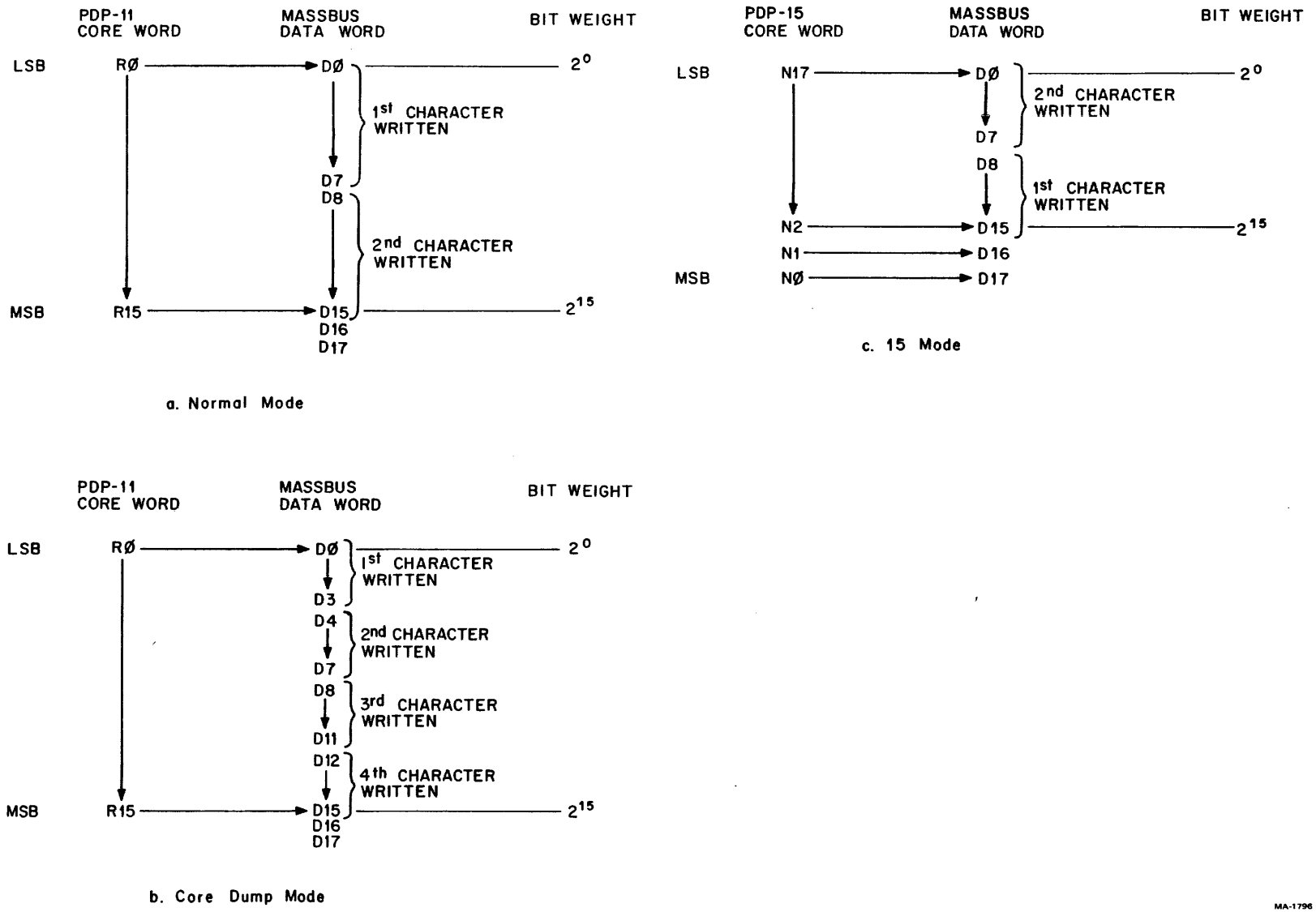


Figure 4-60 M8906 Bit Fiddler Write Formats

Table 4-12 Bit Fiddler Initialization/Operation

Format Mode	Select A		Select B	
	Initial	Toggled by	Initial	Toggled by
Normal Mode	Clear	Toggling inhibited	Clear	WRT STRB
Core Dump	Clear	WRT STRB	Clear	Alternate WRT STRB
PDP-15 Mode	Clear	Toggling inhibited	Set	WRT STRB

4.2.13.3 Bit Fiddler Timing - When WRT STRB H pulses are received by the bit fiddler, it begins disassembling the data word stored in the write buffer. In NRZI mode, this occurs immediately after the start motion delay, when the slave transport is up to speed and transmits WRT CLK to the TM03. In PE mode, WRT STRB pulses are generated after the preamble has been written.

WRT STRB H is generated on the tape control common mode module (TCCM4). When DRV SET PLS H is asserted during a write data operation, the write data record flip-flop is set, generating WDR H. In NRZI mode (PESB L negated), this enables generation of WRT STRB H when WRT CLK is produced by the slave transport. WRT STRB and WRT CLK will be at the same frequency. In PE mode, WRT STRB H is also derived from WRT CLK; however, PE WRT ENABLE L and DATA CLK H must be asserted. This occurs when the data portion of a record is written. Because the frequency of DATA CLK H is half that of WRT CLK, WRT STRB H will also be at half the frequency of WRT CLK H (Figure 4-61).

Figure 4-62 is a timing diagram for bit fiddler write operation in core dump mode. Each time a WRT STRB H pulse is generated, the select A and/or select B flip-flops are toggled. The frame count register is also incremented (FCCLK H, BF2) at each WRT STRB H. For each combination of SLCT A and SLCT B, a separate character is multiplexed onto the bit fiddler output lines; this character becomes available to the write circuitry in the TCCM module.

In core dump (or normal) mode, completion of data word disassembly is detected and the MB XFR flip-flop is clocked set. MB XFR H generates an SCLK pulse, which clears the MB XFR flip-flop and is transmitted to the Massbus controller. The controller responds to SCLK with a WCLK pulse which loads the bit fiddler write buffer with the data word on the data lines. The controller then places a new data word on the data lines, places a data parity bit on the DPA line, and waits for the next SCLK pulse. In the meantime, the bit fiddler performs its disassembly process on the new word in its write buffer. When this word is disassembled, another SCLK is transmitted to the controller; this cycle continues until all the data has been transferred.

Each time the write buffer is loaded, a data bus parity check is performed. If there is a parity error, the parity error flip-flop (BF3) is set and SET DPAR H is generated. This causes the DPAR bit in the error register to be set.

If a WRT STRB H pulse occurs before the bit fiddler receives a WCLK response from the Massbus controller, SET DTE L (set drive timing error) is asserted. This causes the DTE bit in the error register to be set.

4.2.13.4 Parity Generation - Each 8-bit data character output from the bit fiddler write multiplexer is applied to a parity tree where a parity bit is generated for the data character. The parity bit plus the eight data bits form the 9-bit data characters applied to the TCCM module (M8933).

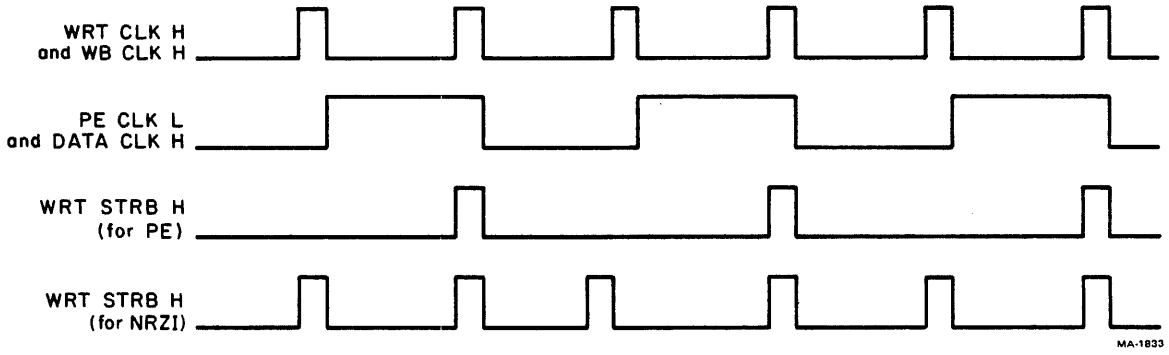


Figure 4-61 WRT STRB Timing

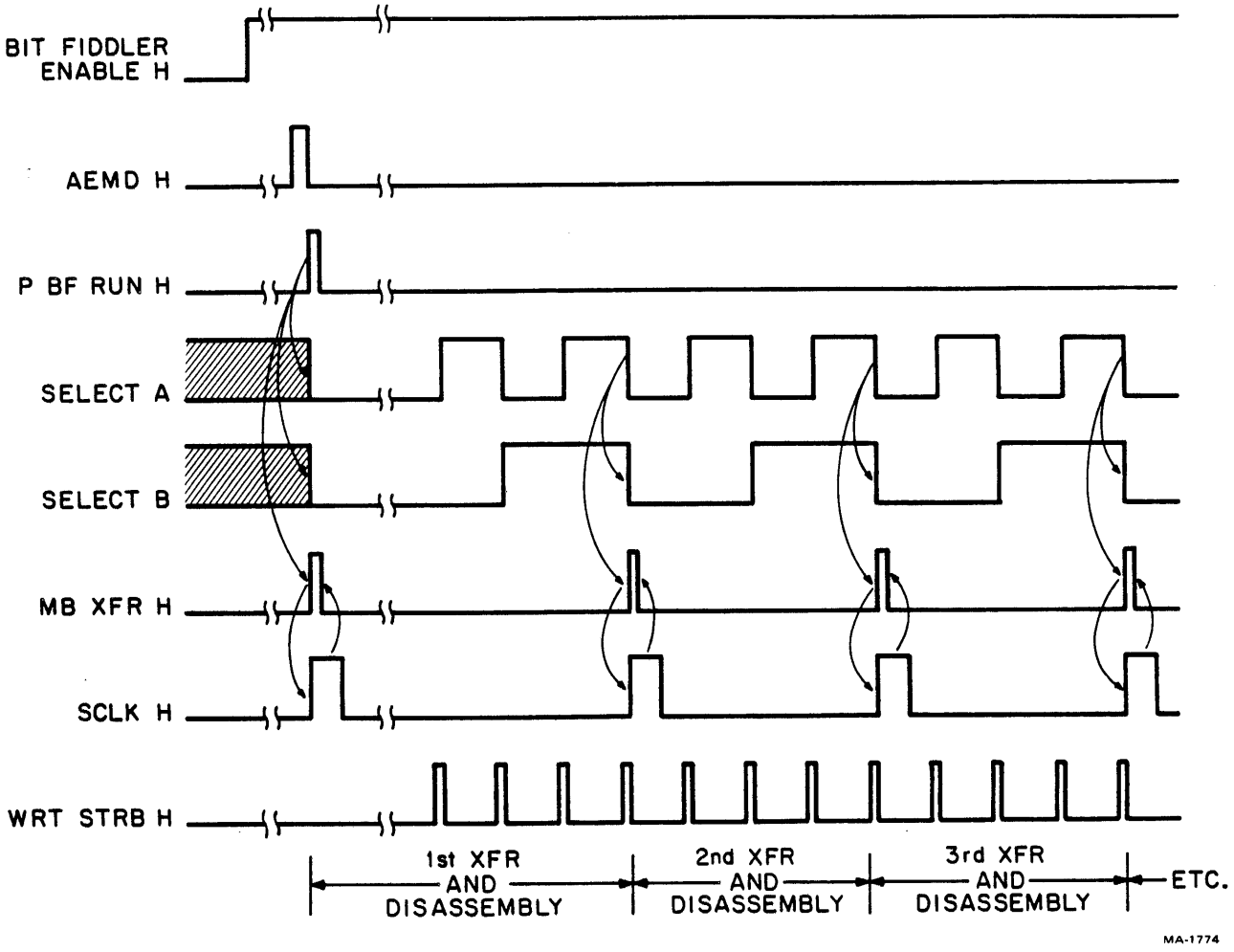


Figure 4-62 Bit Fiddler Write Operation in Core Dump Mode

4.2.14 Power

This paragraph describes the routing of power to and within the TM03. An H740-DA* power supply provides ac and dc power and power-fail logic signals (AC LO and DC LO) to the TM03 (Figure 4-63). An ac cable carries 115 Vac for the TM03 cooling fan. A dc cable connects to the TM03 backplane with ten slip-on fasteners. Voltage levels present on the fasteners are:

+5 V
+15 V
−15 V
GND
AC LO
DC LO

DC power distribution to the TM03 modules is accomplished via the backplane.

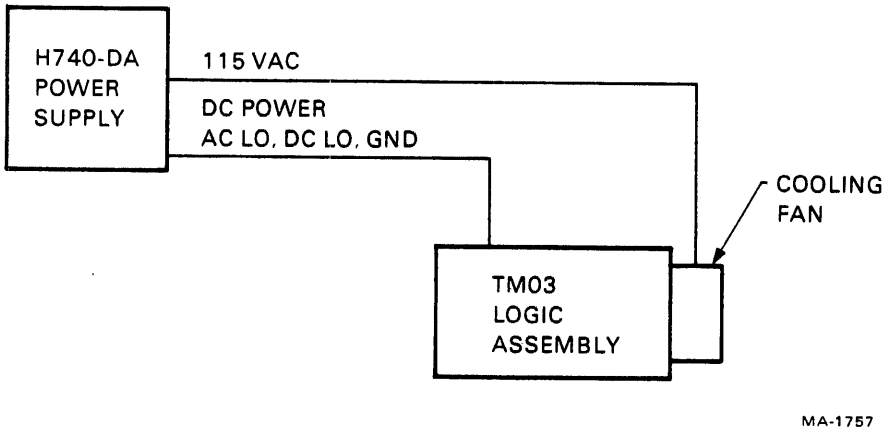


Figure 4-63 TM03 Power System

*Refer to the H740-D maintenance manual listed in Table 1-1. The H740-DA differs from the H740-D power supply in that an ac connector has been added to power the cooling fan in the TM03 housing.

CHAPTER 5
MAINTENANCE

5.1 SCOPE

This chapter provides a complete description of the TM03 preventive and corrective maintenance procedures. The TM03 must operate with a tape transport; however the maintenance instructions provided herein are for the TM03 tape formatter only and do not apply to the transport. Refer to the maintenance manual for the specific transport for transport maintenance instructions. (Table 1-1 lists the manuals for the transports that can be used with the TM03.) Also included in this chapter are power supply adjustments and a description of the various module jumper configurations that will be encountered.

5.2 MAINTENANCE PHILOSOPHY

The TM03 utilizes a "module swap" maintenance philosophy. When troubleshooting, diagnostic programs are run and, if necessary, additional testing is performed, until the faulty module is identified. The error information provided by the diagnostics, when used in conjunction with the diagnostic documentation, indicates the functional area at fault. In some cases the diagnostic indicates which module is at fault. When further testing is required to locate the bad module, use is made of the engineering drawings and the flow and block diagrams in Chapter 4. The TM03 modules are functionally designed so that, in most cases, once the trouble has been localized to a functional area, it has also been localized to a specific module.

5.3 TEST EQUIPMENT

Maintenance procedures for the TM03 require no special tools or test equipment and only a few items of standard equipment. These items are listed in Table 5-1.

Table 5-1 Standard Tools and Test Equipment Required

Equipment	Manufacturer	Designation
Dual-trace oscilloscope	Tektronix	Type 465 or equivalent
Digital voltmeter (capable of reading tenths of volts)	—	—
Trimpot alignment tool (or insulated screwdriver)	—	—
Hex-height module extender	DIGITAL	W904
Diagnostics (MAINDECS)	DIGITAL	See Paragraph 5.8.1

5.4 PREVENTIVE MAINTENANCE

5.4.1 PM Schedule

The PM items listed in Paragraph 5.4.2 are to be performed on a quarterly basis.

5.4.2 PM Checks

5.4.2.1 DC Voltage Check – Check the three dc voltages (+5, +15, -15) from the H740-DA power supply. Make the checks on the TM03 backplane (Figure 5-1). If any of the voltages are outside the tolerances given in Table 5-2, adjust all three voltages according to Paragraph 5.5.

Table 5-2 TM03 DC Voltages

Voltage	Tolerance
+5 V	+0.3, −0 V
+15 V	+0.1, −0 V
−15 V	+0, −0.5 V

5.4.2.2 Fan Check – Ensure that the cooling fan on the front of the TM03 housing operates when power is applied. When the power is removed, the fan should take at least 1 second to come to a stop. If the fan comes to a stop in less than 1 second, the bearings are worn, in which case the fan assembly must be replaced.

5.4.2.3 Diagnostics – Run the complete diagnostic complement for the TM03/transport. Paragraph 5.8.1 lists and describes these diagnostics.

5.5 TM03 ADJUSTMENTS

There are no adjustments in the TM03. The H740-DA power supply has adjustments for the three output voltages supplied to the TM03. To adjust the voltages, remove the cover from the power supply and locate the three adjustment potentiometers (Figure 5-2). Use a well-calibrated digital voltmeter. Connect the voltmeter to the TM03 backplane using Figure 5-1. Using a trimpot alignment tool, or insulated screwdriver, adjust the three potentiometers as follows:

R35 for +15.0 V
R26 for −15.0 V
R50 for +5.0 V

Clockwise adjustment of the potentiometers increases the voltage.

CAUTION

Make adjustments slowly and do not adjust voltages beyond their 105 percent rating to avoid tripping the overvoltage crowbar protection circuit. If the circuit is tripped, dc output fuses will blow.

5.6 MODULE/SYSTEM COMPATIBILITY AND MODULE JUMPERS

5.6.1 Module/System Compatibility

Several TM03 module configurations will occur, depending on which tape transport and processor are used in a particular system. System errors will occur if the modules used are not compatible with the rest of the system. Compatibility must be considered with respect to both the transport and the processor.

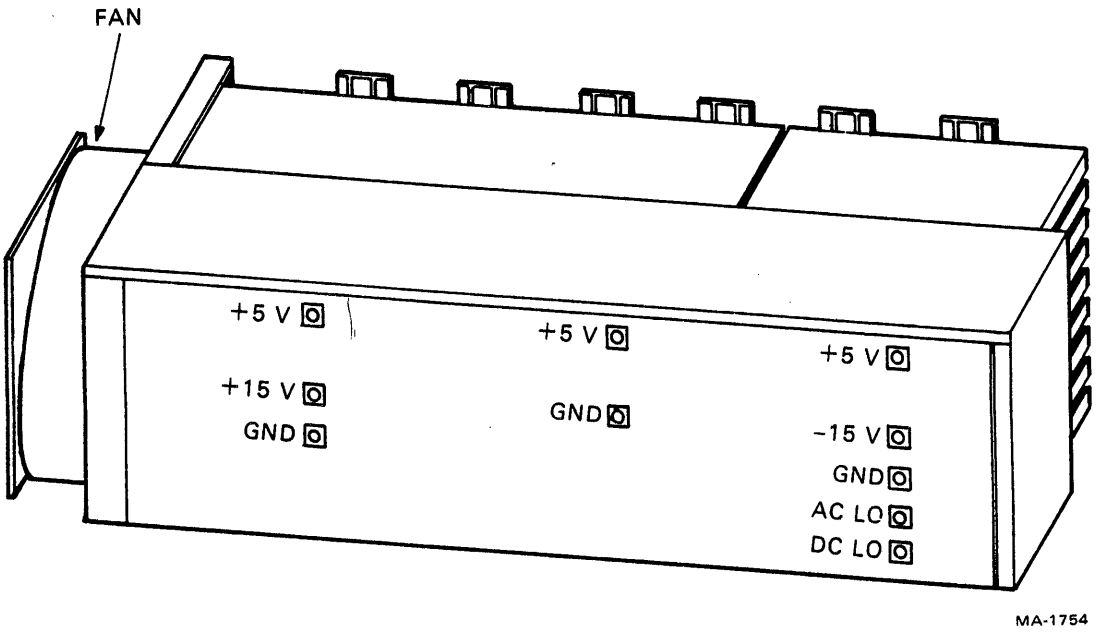


Figure 5-1 DC Voltages on TM03 Backplane

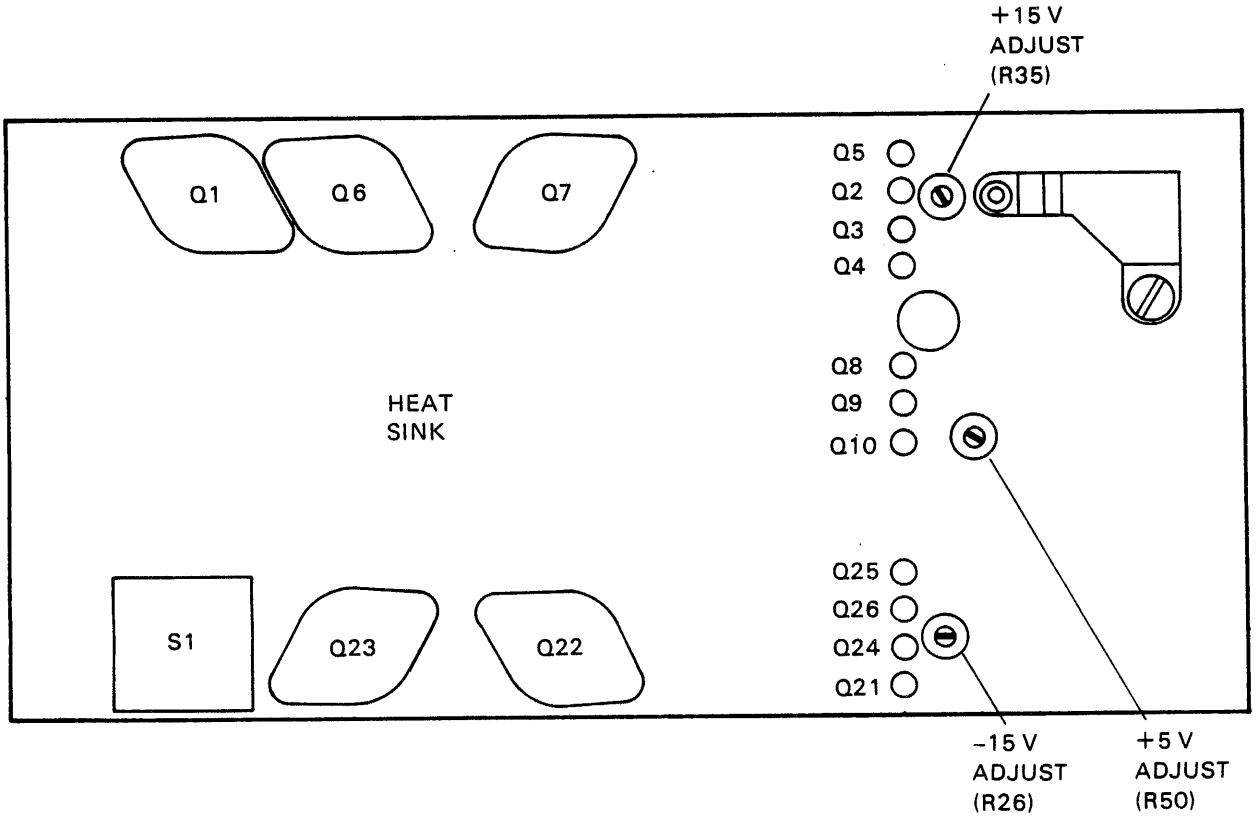


Figure 5-2 H740-DA Power Supply Adjustments

5.6.1.1 Data Sync Modules – All transports connected to a TM03 must be of the same tape speed and the three M8901 data sync modules must be compatible with that speed. That is, the modules must be:

M8901-YBs for 114.3 cm/s (45 in/s) slaves
M8901-YCs for 190.5 cm/s (75 in/s) slaves
M8901-YDs for 317.5 cm/s (125 in/s) slaves.

5.6.1.2 Bit Fiddler Modules – The type of bit fiddler modules used depends on the system processor and the transport tape speed. Ensure that the bit fiddler modules are compatible with the system processor according to Table 5-3. M8915-YA can be used with 114.3 cm/s (45 in/s), 190.5 cm/s (75 in/s), or 317.5 cm/s (125 in/s) transports. M8915 can be used with 114.3 cm/s (45 in/s) or 190.5 cm/ (75 in/s) transports but not with 317.5 cm/s (125 in/s), transports (TU77).

Table 5-3 Bit Fiddler Modules vs System Processor

Bit Fiddler Module	Processor	Processor Word Length
M8906	PDP-11 PDP-15 (normal mode)	16 bits 18 bits
M8915-YA (or M8915) See Paragraph 5.6.1.2	PDP-10 PDP-15 (core dump mode)	36 bits 18 bits

5.6.1.3 NRZI Tape Control Modules – The type of NRZI tape control modules used in slot D-F05 depends on the type of transport. An M8934 is used on 114.3 cm/s (45 in/s) and 317.5 cm/s (125 in/s) transports (TE16 and TU77), while an M8934-YA is used on 190.5 cm/s (75 in/s) transports (TU45).

5.6.2 Module Jumpers

Some of the TM03 modules have provisions for jumper connections. These jumpers must be properly installed for correct TM03 operation. The following paragraphs describe the various jumper configurations.

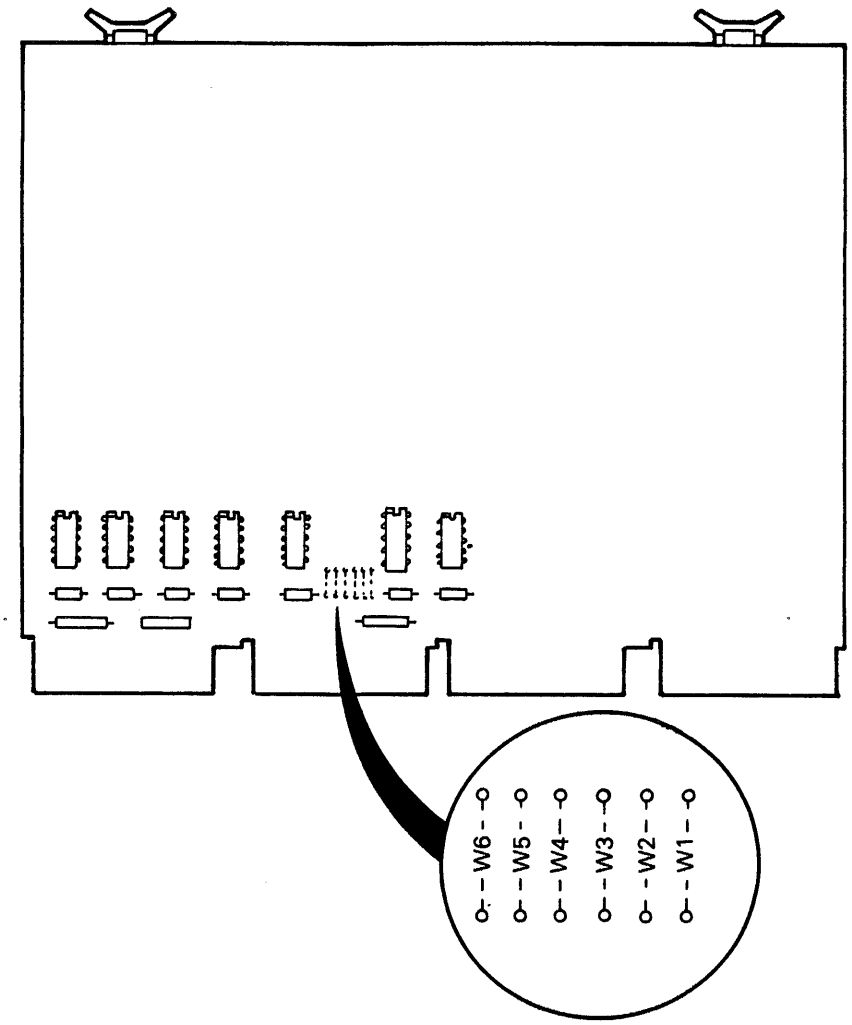
5.6.2.1 PE Data Sync Module (M8901*) – The M8901 series modules have three pairs of jumper terminals (W1-W2, W3-W4, W5-W6) used to identify the module type and to ensure that all three data sync modules are of the correct speed for the slave transport being used. Jumpers are installed onto one pair of terminals according to module type (Figure 5-3). The jumpers form part of a sensing circuit that asserts an NEF error if all three M8901 modules are not matched to the tape speed of the slave transport. (See Paragraph 4.2.6.2 for a description of the error sensing network.)

NOTE

It is important to note that the jumpers merely identify the module type and do not determine its operating speed.

Figure 5-3 illustrates the location of the M8901 jumpers.

*M8901-YB has a speed of 114.3 cm/s (45 in/s)
M8901-YC has a speed of 190.5 cm/s (75 in/s)
M8901-YD has a speed of 317.5 cm/s (125 in/s)



M8901-YB = W1-W2 IN (W3-W4; W5-W6 OUT); 45 IPS SPEED
M8901-YC = W3-W4 IN (W1-W2, W5-W6 OUT); 75 IPS SPEED
M8901-YD = W5-W6 IN (W1-W2, W3-W4 OUT); 125 IPS SPEED

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Figure 5-3 M8901 Jumpers

5.6.2.2 NRZI Tape Control Module (M8934 or M8934-YA) - The NRZI tape control module has three jumpers, W1, W2, and W3 (Figure 5-4). Jumper W1 is normally left out to enable the NRZI error correction feature. (See Paragraph 4.2.8.3 and sheet 2 of Figure 4-39 for a description of the function of W1 in the error correction process.) When W1 is installed, NRZI error correction is inhibited.

NOTE
If W1 is installed, control logic test 2 will produce errors.

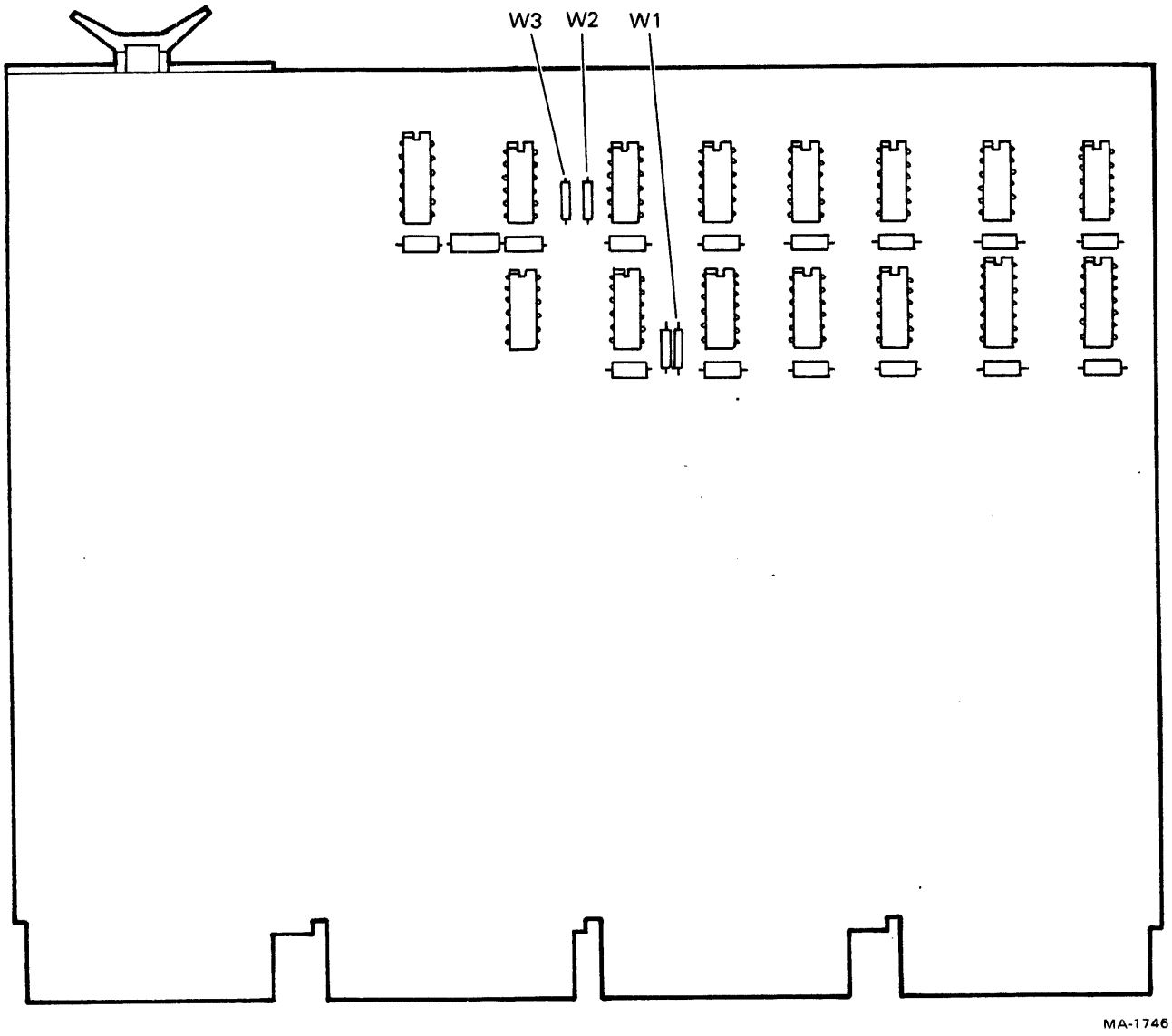


Figure 5-4 M8934 Jumpers

Jumpers W2 and W3 determine the minimum allowable record length in the NRZI mode. The normal configuration (W2 in and W3 out) causes an NEF error when an attempt is made to write an NRZI record of less than ten characters. An ITM error occurs if a record of less than ten characters is read. If it is desired to read records of less than ten characters, W2 is removed and W3 is installed.

NOTE

When the short record capability is enabled (W2 out and W3 in), certain error conditions, such as noise blocks, will not assert an NSG error flag as they normally would.

5.6.2.3 Maintenance Register Module (M8905-YB) – The maintenance register module has one jumper (W1) which is always out for the TM03. Figure 5-5 illustrates the location of the jumper.

Bit 13 of the tape control register, located on M8905-YB, is SAC for the TM03 and TCW for the TM02. One of the steps to change an M8905-YB (TM03) into an M8905 (TM02) is to change bit 13 from SAC to TCW. Jumper W1 accomplishes this step.

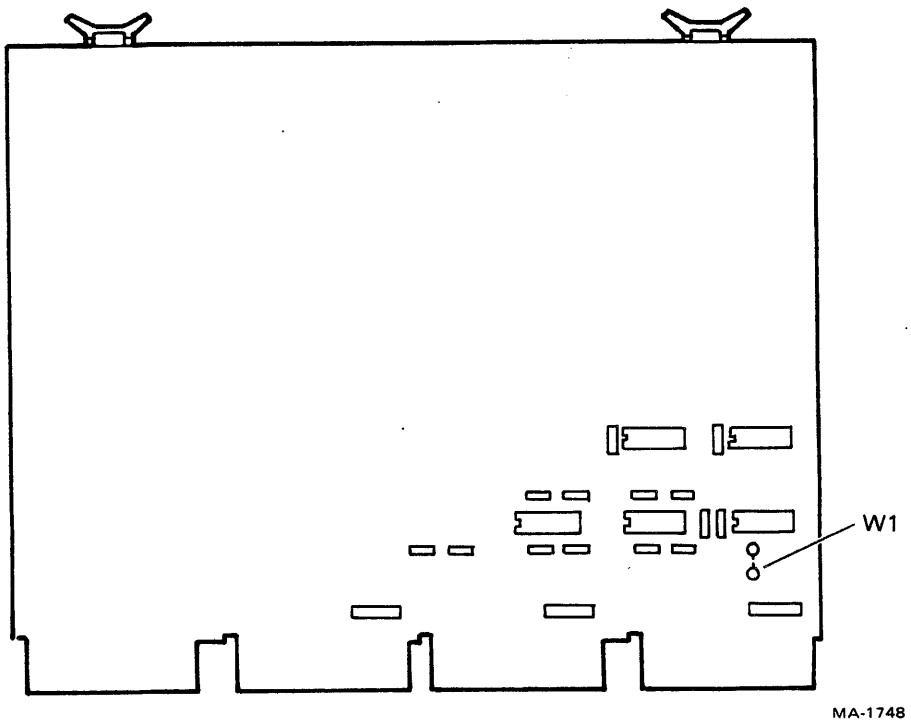


Figure 5-5 M8905-YB Jumper

5.6.2.4 Control and Write Drivers (M8937) – Two jumpers (W1, W2) are located on M8937 and affect the auto density select capability of the TM03. The auto density select feature is enabled when W1 is in and W2 is out. To disable this feature and place density control under control of the DEN 2 bit, remove W1 and install W2.* (Refer to Paragraph 4.2.6.1 and Figure 4-28 for a discussion of the auto density select process.) Figure 5-6 illustrates the location of the jumpers.

5.7 REMOVAL AND REPLACEMENT

There are no removal and replacement procedures required for the TM03 tape formatter. The TM03 is made up of 15 modules, enclosed in a housing with a cooling fan mounted on the front of the housing. The modules are simply removed or inserted as required. The fan on the front of the housing is removed via four mounting screws. Figure 5-7 illustrates the location of the TM03 modules.

*A jumper change is also required in the slave transport.

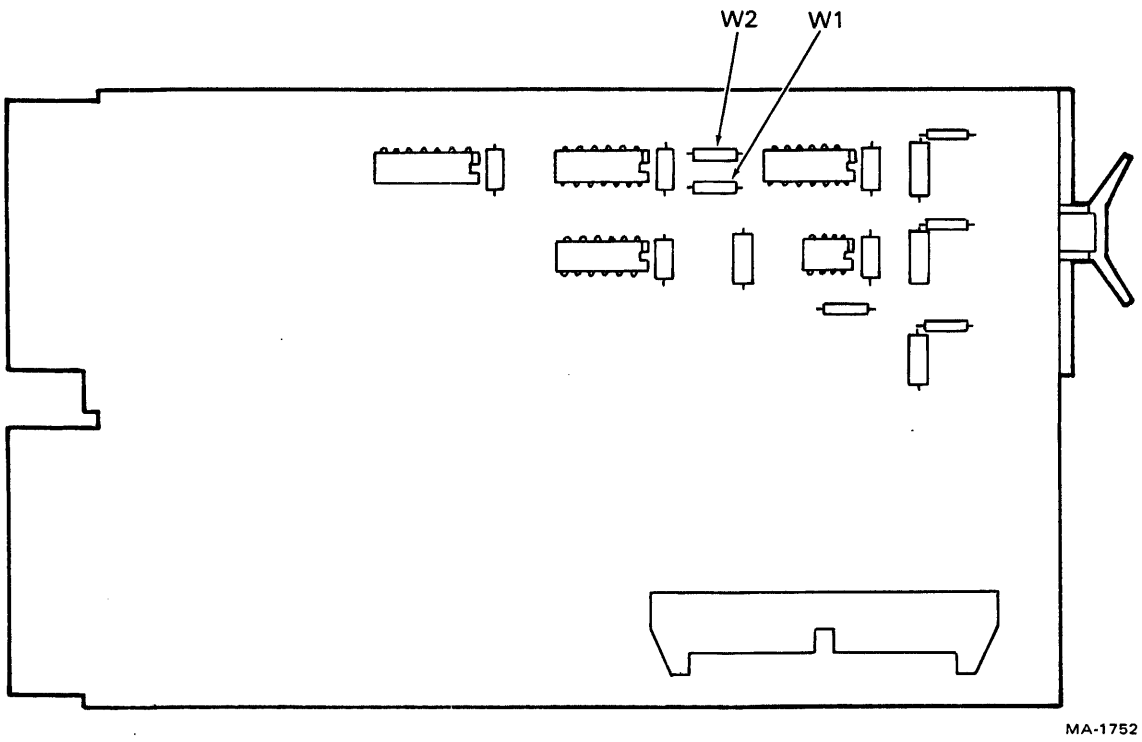
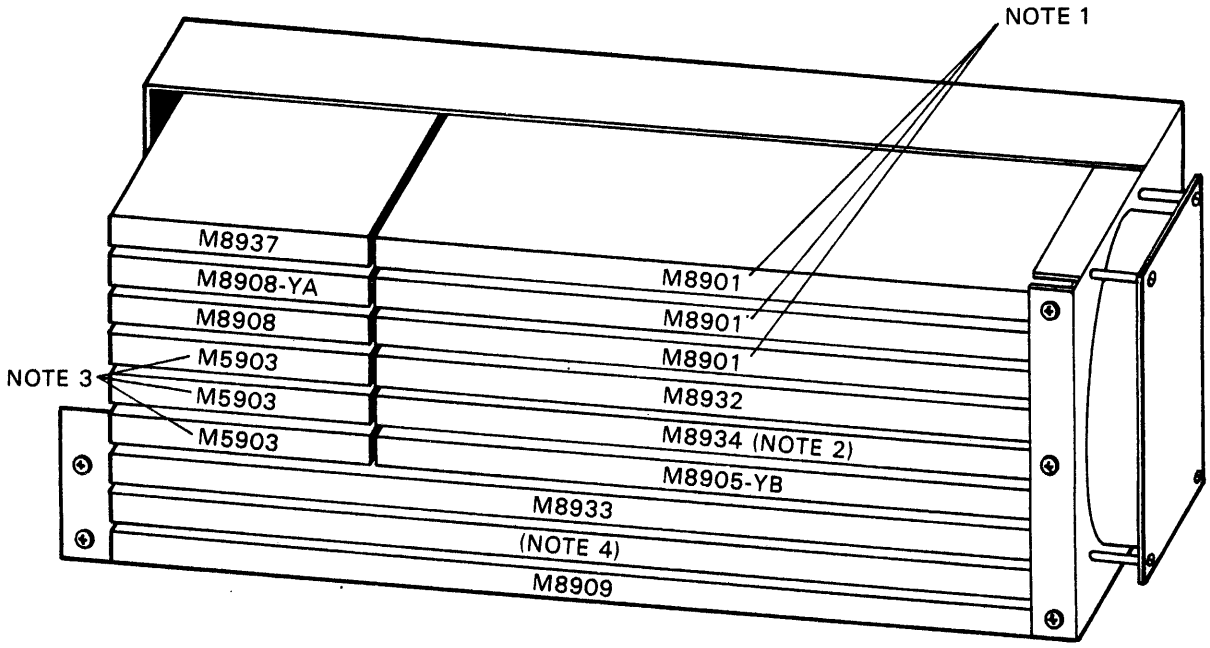


Figure 5-6 M8937 Jumpers



NOTES

1. M8901-YB FOR TE16 (45 IPS)
   M8901-YC FOR TU45 (75 IPS)
   M8901-YD FOR TU77 (125 IPS)

2. M8934 FOR TE16 AND TU77
   M8934-YA FOR TU45

3. MAY BE M5903 OR M5903-YA

4. M8906 WHEN CPU IS PDP-11
   M8915-YA WHEN CPU IS PDP-10 AND TRANSPORT IS TU77
   M8915 OR M8915-YA WHEN CPU IS PDP-10 AND TRANSPORT IS TE16 OR TU45.

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Figure 5-7 Location of TM03 Modules

5.8 CORRECTIVE MAINTENANCE

This paragraph covers all the diagnostic test routines used with the TM03. Also provided is trouble analysis and diagnostic information applicable to functional areas of the TM03.

5.8.1 Diagnostics

The TM03 cannot function independent of a slave transport. It must be connected to a slave to obtain required clock signals. Consequently, most of the diagnostics treat the TM03 and the transport as a subsystem* with each subsystem variation having its own set of diagnostics. Table 5-4 lists the diagnostics used with TE16, TU45, and TU77 transports for both a PDP-11 system and PDP-10 system.

The two control logic test diagnostics specifically test the TM03 and can isolate certain troubles to a specific module. The diagnostic documentation has complete instructions on how to run the control logic test and how to interpret the results.

The remaining diagnostics localize trouble to a functional area instead of a module. In some cases, additional tests and analyses must be made to isolate between the TM03 and the transport and then to identify the faulty module. Instructions on how to run these diagnostics and interpret the results can be found in the maintenance manual of the specific transport. (See Table 1-1 for a list of transport maintenance manuals.)

While troubleshooting the TM03, it is important to note that the control logic test diagnostics may run satisfactorily while the data reliability diagnostic fails. The control logic tests use the maintenance clock when checking the data and control paths. The frequency of the maintenance clock is a function of transport speed; however for a given transport speed the clock runs at a constant rate; therefore marginal components and modules in the TM03 perform satisfactorily. When running the multidrive data reliability diagnostic (or other system software) the TM03 clock becomes a function of the transport data read rate. Certain transport irregularities, such as jitter and dynamic skew, cause the clock to run at an irregular rate, causing the same marginal components or modules to produce errors. (An area of the TM03 particularly susceptible to this type of marginal operation is the three M8901 data sync modules which contain the phase lock loops for reading PE data.) Thus the control logic tests may be used for troubleshooting but system performance must be verified using the multidrive data reliability diagnostic.

5.8.2 Clock Trouble Analysis

1. Run the drive function timer diagnostic.

   There should be no out-of-range errors. (The diagnostic may fail for reasons other than faulty clocks.) Use the diagnostic printout for trouble analysis.

2. With a transport selected, loaded, and on-line, connect an oscilloscope to pin F06S1 on the TM03. Check for a clock square-wave (TAPE SPEED CLK) of the following frequency:

   114.3 cm/s (45 in/s) transport = 9.00 kHz (period = 111 μs)
   190.5 cm/s (75 in/s) transport = 7.50 kHz (period = 133 μs)
   317.5 cm/s (125 in/s) transport = 6.25 kHz (period = 160 μs)

3. Use Figures 5-8 and 5-9 as a guide for trouble analysis of TM03 clock signals

*The exception is the Data Tape Create diagnostic MAINDEC-11-DZTUF which does not require the use of a tape transport.

Table 5-4 TM03/Transport Diagnostics

Processor	Title	Transports			Description
		TE16	TU77	TU45	
PDP-11	Multidrive Data Reliability	MAINDEC-11-DZTED	MAINDEC-11-DZTED*	DECSPEC 11-BDHDD	Tests TM03 and transport circuitry by writing and reading user-determined or pre-determined data patterns and recording modes. Provides error information to the user via the console.
	Basic Function Test	MAINDEC-11-DZTEC	MAINDEC-11-DZTEC*	DECSPEC 11-BDHCD	Tests the subsystem command functions (read, write, space, etc.).
	Control Logic Test 1	MAINDEC-11-DZTEA	MAINDEC-11-DZTEA*	DECSPEC 11-BDHAD	Tests TM03 logic. Includes control and data logic in maintenance modes wrap 0 through 3. Indicates probable faulty area.
	Control Logic Test 2	MAINDEC-11-DZTEB	MAINDEC-11-DZTEB*	DECSPEC 11-BDHBD	Test TM03 logic. Includes control and data logic in maintenance mode wrap 4. Indicates probable faulty area.
	Drive Function Timer	MAINDEC-11-DZTEE	MAINDEC-11-DZTEE*	DECSPEC 11-BDHED	Tests for proper tape motion timing (speed, acceleration, deceleration) and data transfer rate.
	Utility Driver (Brutis)	MAINDEC-11-DZTEF	MAINDEC-11-DZTEF*	DECSPEC 11-BDHFD	A brute force routine that performs up to 15 operational functions determined by the user.
	Data Tape Create	MAINDEC-11-DZTUF	MAINDEC-11-DZTUF	-	A utility program supplement to the multidrive data reliability diagnostic. Creates a paper tape containing a desired data pattern for use as pattern 0 of the random data exerciser portion of the multidrive data reliability diagnostic.

*Revision B or higher.

Table 5-4 TM03/Transport Diagnostics (Cont)

Processor	Title	Transports			Description
		TE16	TU77	TU45	
PDP-11/780 VAX	Data Reliability	ZZ-ESMAA	ZZ-ESMAA	-	Test TM03 and transport circuitry by writing and reading user-determined or pre-determined data patterns and recording modes. Provides error information to the user via the console.
	Drive Function Timer	ZZ-ESMAB	ZZ-ESMAB	-	Tests for proper tape motion timing (speed, acceleration, deceleration) and data transfer rate.
DECsystem-10/20 with RH10	Basic and Reliability Diagnostic	MAINDEC-10-DDTUG†	-	MAINDEC-10-DDTUG†	This diagnostic tests multiple drives serially. It runs one drive through a group of tests and then runs the next drive through the same tests.
	Magtape Reliability Diagnostic	MAINDEC-10-DDTUK	-	MAINDEC-10-DDTUK	Performs reliability tests in the area of interchange read/write, compatibility, and operator function select.
DECsystem-10/20 with RH20	Magtape Basic/ Reliability Diagnostic	MAINDEC-10-DFTUE‡	MAINDEC-10-DFTUE**	MAINDEC-10-DFTUE‡	Includes read and write retry testing of the tape formatter and the slave transport.
	Magtape Reliability Diagnostic	MAINDEC-10-DFTUK	MAINDEC-10-DFTUK*	MAINDEC-10-DFTUK	Performs reliability tests in the area of interchange read/write, compatibility, and operator function select.

* Revision B or higher.
† Revision C or higher
‡ Revision E or higher
** Revision F or higher

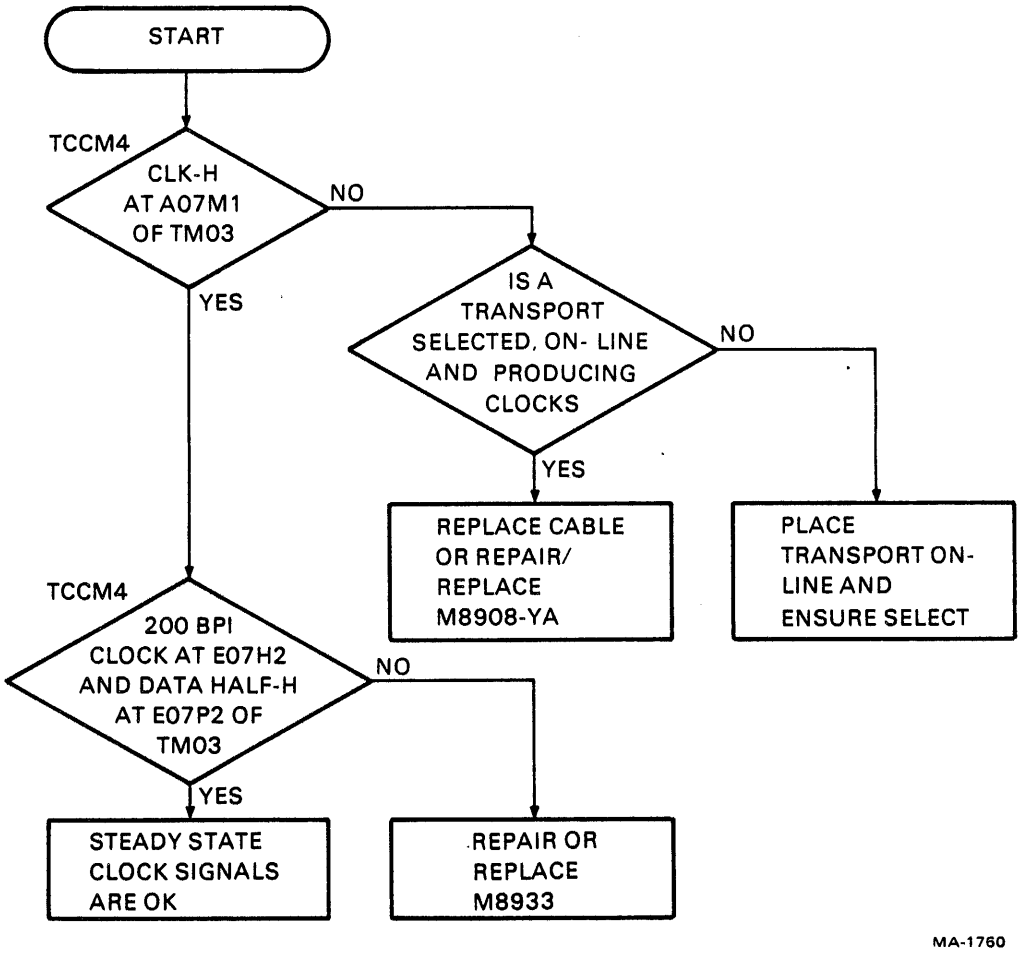


Figure 5-8 Steady State Clock Trouble Analysis

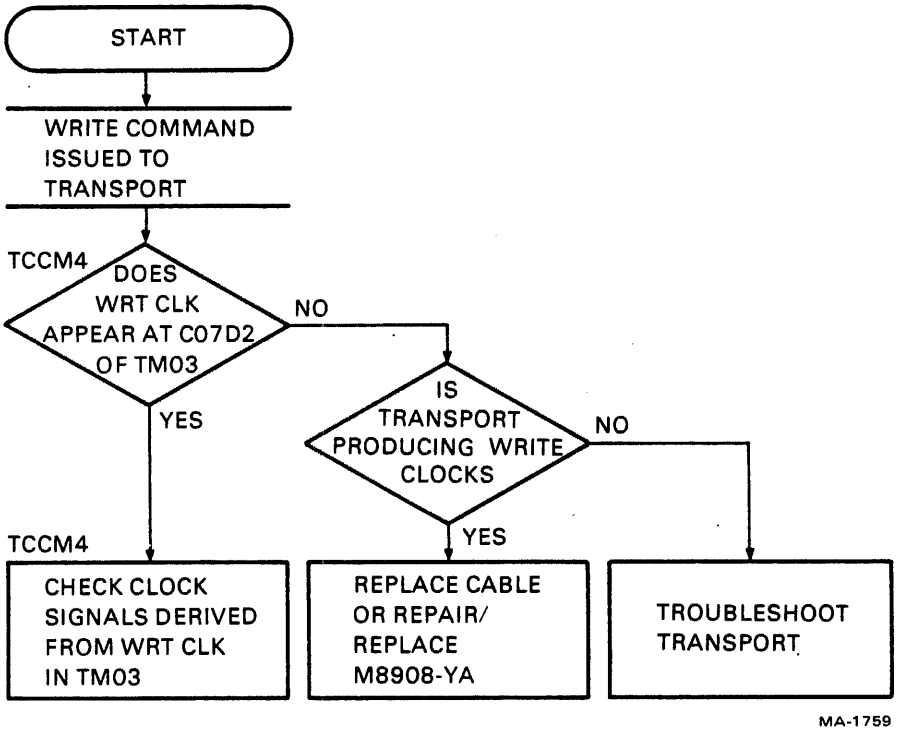


Figure 5-9 Write Clock Trouble Analysis

5.8.3 Register Read/Write Trouble Analysis

1. Run the control logic test diagnostics. Use the diagnostic documentation for trouble analysis.

2. Refer to flowcharts in Figures 4-17 and 4-19, and the timing and block diagrams of Figures 4-18, 4-20, 4-21, and 4-22.

3. Use Table 5-5 as a guide for trouble analysis of register read/write signals.

5.8.4 Error Detection Trouble Analysis

1. Table 5-6 lists errors which could occur during various operations and remain asserted after the operation is completed. If errors other than those indicated occur, the error detection circuitry may be at fault.

2. Run the control logic test diagnostics to locate malfunctioning error detection circuitry. The diagnostics check the operation of each error bit except UNS. The assertion of UNS may be caused by the H740-DA power supply or the loss of MOL from the tape transport.

NOTE
If W1 on module M8934 (or M8934-YA) is installed, the NRZI error correction feature is inhibited and control logic test 2 will produce errors.

Table 5-5 Register Read/Write Trouble Analysis

Symptom	Check for
Massbus controller sets NED, or constant MCPE errors.	• Software selecting proper TM03 address. • Proper TM03 address getting to TM03 and being acknowledged (Is E8-3 on M8909-YA high? MBI2.) • Demand getting to TM03. (Is DEM H asserted at pin A09U2?)
ILR bit sets.	• Register select lines and register select decoder (E14 on M8909-YA; MBI 2)
Data in register read incorrectly without CPAR error.	• Problem with C multiplexer lines, C-line latches, or register flip-flops.
Data in register read incorrectly with CPAR error.	• Massbus cables and transceivers (at TM03 and controller). • No –15 Vdc at controller.
Access to only every second register.	• One bit high on RS lines (MBI2).

Table 5-6 Possible Errors During TM03/Transport Operations

Operations \ Errors	ILF	ILR	RMR	CPAR	FMT	DPAR	INC/VPE	PEF/LRC	NSG	FCE	CS/ITM	NEF	DTE	OPI	UNS	COR/CRC
Write to any register*		X	X	X												
Read from any register		X														
Load CS1 with "NO-OP"	X	X	X	X								X			X	
Load CS1 with "REWIND-OFF LINE"	X	X	X	X								X			X	
Load CS1 with "REWIND"	X	X	X	X								X			X	
Load CS1 with "DRIVE CLEAR"	X	X	X	X											X	
Load CS1 with "WRITE TAPE MARK"	X	X	X	X			X	X	X		X	X		X	X	
Load CS1 with "ERASE"	X	X	X	X							X	X			X	
Load CS1 with "SPACE FWD"	X	X	X	X						X		X		X	X	
Load CS1 with "SPACE REV"	X	X	X	X						X		X		X	X	
Load CS1 with "WRITE CHECK FWD"	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X
Load CS1 with "WRITE CHECK REV"	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X
Load CS1 with "WRITE FWD"	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Load CS1 with "READ FWD"	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X
Load CS1 with "READ REV"	X	X	X	X	X		X	X	X	X	X	X	X	X	X	X
MASSBUS INIT															X	
Write into AS or MR register		X		X												

*Except AS or MR.

3. When troubleshooting the error detection circuitry, it is preferable to start at the error register and work back. Most of the error register flip-flops are located on the Massbus interface module (M8909-YA; MBI 11). The flip-flops not on the interface module are located as follows:

   a. INC/VPE, PEF/LRC, and COR/CRC are on TCPE2/CNRZ3.

   b. CS/ITM is on TCPE2/CNRZ2.

   c. NSG is on TCCM5.

4. If the short record read capability is enabled (W2 out and W3 in on M8934), certain error conditions, such as noise blocks, will not assert NSG as they normally would.

5. Use Table 5-7 as a guide in analyzing errors related to the Massbus controller, Massbus cabling, software, and the H740-DA power supply.

6. Use Table 5-8 as a guide for trouble analysis of tape read/write errors.

7. Use Table 5-9 as a guide for trouble analysis of data errors.

5.8.5 Tape Motion Trouble Analysis

Most tape motion failures occur in the tape transport and are located by off-line troubleshooting of the transport. To check on-line performance, run the following diagnostics in the order listed.

1. Basic function test
2. Control logic test 1
3. Control logic test 2
4. Drive function timer
5. Multidrive data reliability

If the failure is not repeatable due to tape runaway or OPI errors, the utility driver diagnostic should be run.

5.8.6 Data Read/Write Circuits Trouble Analysis

1. Use the multidrive data reliability diagnostic to check out the TM03 read/write circuitry. The acceptable soft error rate is a transport parameter and reference should be made to the applicable transport maintenance manual.

2. If the multidrive data reliability diagnostic fails, use the control logic test diagnostics to troubleshoot the TM03. (Refer to Paragraph 4.2.1 for a description of the maintenance wrap-around modes used by the control logic test diagnostics.)

5.8.7 Bit Fiddler Error Analysis

The bit fiddler (M8915-YA or M8915) contains an LED which is mounted near the handle. Should the LED illuminate during program execution or in idle mode, it is indicative of a bad microcontroller ROM (ROM parity error) and the module should be replaced.

Table 5-7 Massbus Controller, Massbus Cable, Software, and Power Supply Error Analysis

Error	Bit	Mnemonic	Manual Reference Table No.	Print Reference	Control Logic* Test #1; Test No.
Illegal Function	00	ILF	2-4	Set IFL Logic: (MB15, MB17); ILF flip-flop (MBI11); ILF multiplexer (MBI10)	Test 20
Illegal Register	01	ILR	2-4	Register select lines (MB1, MB2); Register select logic (MBI2); ILR flip-flop (MBI11)	Test 27
Register Modification Refused	02	RMR	2-4	RMR logic (MBI2): RMR flip-flop (MBI11) RMR multiplexer (MBI10)	Test 21
Control Bus Parity	03	CPAR	2-4	C lines (MBI1, MBI2, MBI3; CPAR flip-flop (MBI11); C bus multiplexer (MBI3, MBI4, MBI5, MBI8, TCCM7, MR2 through MR6)	Test 3
Format Error	04	FMT	2-4	Format bits (MR6); ILF decode(BF3)	Test 23
Data Bus Parity	05	DPAR	2-4	Parity tree (BF3); DPAR flip-flop (MBI11); C lines (MBI1, MBI2, MBI3)	Test 24
Non-Executable Function	11	NEF	2-4	Analyze program to determine which of five causes are the most probable. Logic decoding of conditions is on MBI7.	Test 25
Drive Timing Error	12	DTE	2-4	Caused by failure in SYNC CLK/ WCLK sequence (BF2) or occupied line (MBI7).	Test 30
Unsafe	14	UNS	2-4	MOL not present (MBI7); H740-DA AC LO is asserted.	Not tested

*PDP-11 systems only. Refer to PDP-10 diagnostic documentation for applicable tests.

Table 5-8 Tape Read/Write Error Analysis

Error	Bit	Mnemonic	Symptom	Probable Cause
Operation Incomplete	13	OPI	–	No data written on tape. No SET PLS. Read logic failure.
Frame Count Error	09	FCE	During a read operation no other error register bits are set.	The Massbus controller was expecting a longer record. This is normal when tape format is unknown.
			In the NRZI mode, during a read or write operation, other data error bits are present.	Usually indicates the read amp output changed during the skew over pulse. Verify signal amplitudes and tape speed.
			Errors occur only during a write operation.	Usually indicates tape error caused early detection of postamble.

Table 5-9 Analysis of Data Errors*

Mode of Operation	Symptom	Probable Cause
NRZI	PEF/LRC error only	The LRC character or the LRC checking logic is at fault.
	VPE with FCE error	The trouble could be a badly damaged tape, poor velocity regulation, a worn head or a faulty read amplifier.
	CRC and LRC errors without VPE while in the forward direction.	Problem is in the CRC character.
PE	CS/ITM error and NRZI runs	Indicates a problem in detecting the end of the preamble in one or more tracks.
	INC without any bits being set in the CK register	Intermittent deskew channel in the TM03.

*Troubleshoot data errors (INC/VPE, PEF/LRC, COR/CRC, CS/ITM) using Paragraph 5.8.6.

APPENDIX A
GLOSSARY

Mnemonic	Meaning
ACCL	Acceleration
ADDR	Address
AEMD	Acceleration Enable Motion Delay
ANSI	American National Standards Institute
AS	Attention Summary
ASYC WRT	Asynchronous Write
ATA	Attention Active
ATTN	Attention
BCD	Binary Coded Decimal
BF	Bit Fiddler
BFFMTE	Bit Fiddler Format Error
BOT	Beginning of Tape
BPI	Bits Per Inch
7CH	7 Channel
CHK CHAR	Check Character
CK	Check Character
CLK	Clock
CLR	Clear
CMB PE	Control Massbus Parity Error
CNRZ	Tape Control NRZ
CNTR	Counter
CO	Carry Out
COMPER	Composite Error
COR	Correctable Data Error
CPA	Control Bus Parity
CPAR	Control Bus Parity Error
CPI	Characters Per Inch
CPU	Central Processor Unit
CRC	Cyclic Redundancy Check
CRCC	Cyclic Redundancy Check Character
CRCE	Cyclic Redundancy Check Error
CRCS	Cyclic Redundancy Check Strobe
CS	Control Status or Correctable Skew
CT	Count
CTOD	Controller to Drive
CWD	Control and Write Driver
DD TRK	Dead Track
DECL	Decelerate
DEM	Demand
DEN	Density

GLOSSARY (Cont.)

Mnemonic	Meaning
DIP	Dual In-Line Package
DPA	Data Parity
DPA TM	Data Parity Transmit
DPAR	Data Bus Parity Error
DPR	Drive Present
DRQ	Drive Request Required
DRV	Drive
DRY	Drive Ready
DS	Drive Status, Drive Select, or Data Sync
DT	Drive Type or Dead Track
DTE	Drive Timing Error
DVA	Drive Available
EAODTE	Enable Abort on Data Transfer Errors
EBL	End of Block
EMD	Enable Motion Delay
ENB	Enable
ENBL	Enable
END PT	End Point
ENV	Envelope
EOR	End of Record
EORS	End of Record Strobe
EOT	End of Tape
EPR	Error Pattern Register
ER	Error
ERDS	Enable Read Strobe
ERR	Composite Error
EV PAR	Even Parity
EXC	Exception
F	Function
FC	Frame Count
FCCLK	Frame Count Clock
FCE	Frame Count Error
FCS	Frame Count Status
FMK	File Mark
FMT	Format Error
FMT SEL	Format Select
FWD	Forward
ID	Identification
IDB	Identification Burst
ILF	Illegal Function
ILR	Illegal Register
INC	Incorrectable Data Error
INC ERROR	Incorrectable Error
INC PREAMBLE	Incorrect Preamble
ILCC	Illegal Check Character
INIT	Initialize
IPS	Inches Per Second
IRD	Interchange Read
IRG	Interrecord Gap
ITM	Illegal Tape Mark
LCTOD	Load Controller to Drive
LRC	Longitudinal Redundancy Check

GLOSSARY (Cont.)

Mnemonic	Meaning
LRCC	Longitudinal Redundancy Check Character
LRCS	Longitudinal Redundancy Check Strobe
LSB	Least Significant Bit
(M)	TM03 Logic
MB	Massbus
MB XFR	Massbus Transfer
MBI	Massbus Interface
MC	Maintenance Clock
MCPE	Massbus Control Bus Parity Error*
MDF	Maintenance Data Field
MM	Maintenance Mode
MMEOR	Maintenance Mode End of Record
MOH	Moving Head
MOL	Medium on Line
MOP	Maintenance Operation Code
MR	Maintenance Register
MSB	Most Significant Bit
MTA	Magnetic Tape Adapter
NED	Nonexistent Drive*
NEF	Non-Executable Function
NRZI	Non Return to Zero Inverted
NSA	Not Sector Addressed
NSG	Non-Standard Gap
OCC	Occupied
OCC TM	Occupied Transmit
OP	Operation
OPI	Operation Incomplete
P BF RUN	Preset Bit Fiddler Run
PAR	Parity
PE	Phase Encoded
PEF	Phase Encoded Format Error
PERR AND ONE DD TRK	Parity Error and One Dead Track
PES	Phase Encoded Status
PESB	Phase Encoded Status Buffered
PIP	Positioning in Progress
PLS	Pulse
POS	Postamble
POST PAT	Postamble Pattern
PRE	Preamble
PREVER	Previous Error
R	Register
RD	Read Data or Read
RDS	Read Strobe
REC	Record
REG	Register
REV	Reverse
RMR	Register Modification Refused
RS	Register Select or Reset
RSDO	Read Strobe Delay Over
RST	Reset
RWND	Rewind
RWS	Rewind Status

*Controller signal.

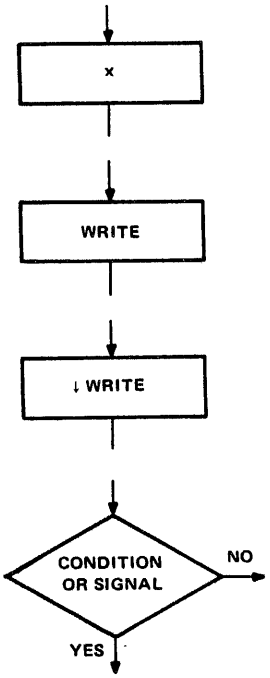
GLOSSARY (Cont.)

Mnemonic	Meaning
(S)	Any Transport
SAC	Slave Address Change
SB	Slave Bus
SCLK	Sync Clock
SDWN	Settle Down
SEL	Select
SHDN	Shutdown
SHDWN	Shutdown
SLA	Slave Attention
SLCT	Select
SN	Serial Number
SPR	Slave Present
SS	Slave Select
(SS)	Selected Transport
SSC	Slave Status Change
ST CLK	State Clock
STRB	Strobe
SWC	Selected Slave Clock
TAP	Tape Drive
TC	Tape Control
TCCM	Tape Control Common Mode
TCPE	Tape Control Phase Encoded
TM	Tape Mark
TMRK	Tape Mark
TMWIP	Tape Mark Write in Progress
TPMK	Tape Mark
TRA	Transfer
TRANS	Transition
TRK n* ERR	Track n* Error
TUR	Tape Unit Ready
UNS	Unsafe
VCO	Voltage Controlled Oscillator
VPAR	Vertical Parity Error
VPE	Vertical Parity Error
VRC	Vertical Redundancy Check
WB CLK	Write Buffer Clock
WCLK	Write Clock
WD	Write Data
WDBFO	Write Data Bit Fiddler Output
WDR	Write Data Record
WDWBO	Write Data Write Buffer Output
WFMK	Write File Mark
WRL	Write Lock
WRP	Wraparound
WRT CLK	Write Clock
WTMK	Write Tape Mark

*n = track number

APPENDIX B

FLOWCHART GLOSSARY



x = Description of an event or action (lower case).

The signal level WRITE is asserted.

The signal level WRITE is negated.

If condition or signal is true flow follows YES branch, otherwise flow follows NO branch.

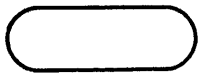
A flip-flop is set asserting WRITE.

A flip-flop is reset negating WRITE.

Delay. If delay is fixed x = amount of delay or delay range.

Off page connector.

On page connector.



Beginning or ending point of a flow diagram.

11-4781

APPENDIX C
RECORDING TECHNIQUES

C.1 NRZI (Non-Return to Zero Inverted)

C.1.1 Definition

NRZI is a recording technique which requires a change of state (flux change) to write a 1, and no change of state (no flux change) to write a 0.

C.1.2 Format

Cyclic Redundancy Check Character (CRCC) – This is a check character that is written four character spaces after the last character of an NRZI record (9-channel only). CRCC is derived by a complex mathematical formula applied to the characters written in the record. The result of this manipulation (CRCC) can be used to recover a lost bit in a record read from tape.

Longitudinal Parity Check Character (LRCC) – This check character is written four character spaces after CRCC (9-channel). LRCC consists of one bit of even parity for each track of data. For example, if track 1 had an odd number of 1s written in a record, then a 1 must be written in the LRCC bit associated with track 1.

Tape Mark – A 9-channel NRZI tape mark consists of one tape character (23_8), followed by seven blank spaces, and then LRCC (23_8). (CRCC is not written.) Figure C-1 illustrates 9-channel NRZI tape format.

C.2 PE (Phase Encoding)

C.2.1 Definition

Phase encoding is a recording technique in which a flux reversal occurs for each bit of information written on the tape. A 1 can be defined as a positive level followed by a negative transition, while a 0 can be defined as a negative level followed by a positive transition.

Sequential flux transitions on the tape are either at the data rate or at twice the data rate. Sequential 1s or sequential 0s will cause flux reversals to occur at twice the data rate (Figure C-2a). Alternate 1s and 0s cause flux reversals to occur at the data rate (Figure C-2b).

C.2.2 Format

To ensure proper extraction of PE data from the serial stream of transitions coming off the tape, PE data must be recorded in a precise format. A PE record consists of preamble, data, and postamble.

1. Preamble: Forty characters of 0s in all nine tracks, followed by a character of 1s in all nine tracks.

2. Postamble: One character of 1s in all nine tracks, followed by 40 characters of 0s in all nine tracks.

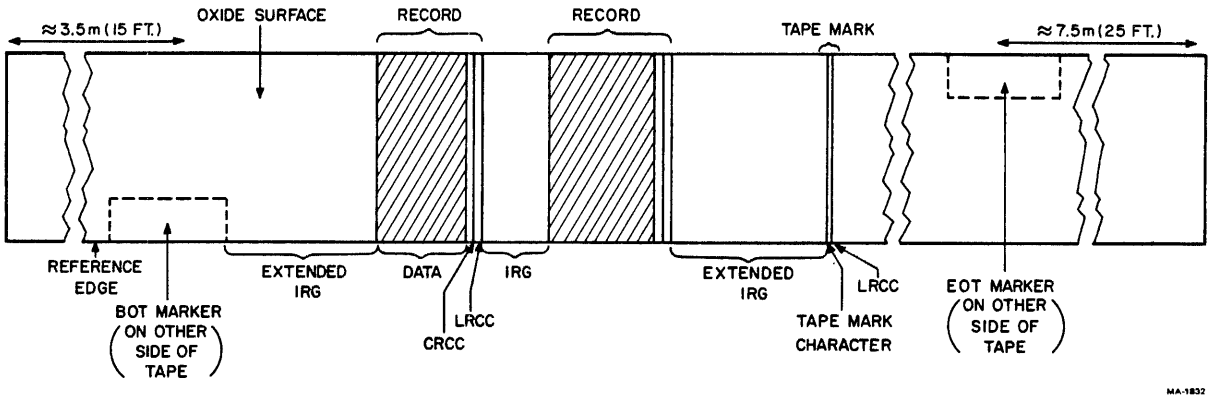
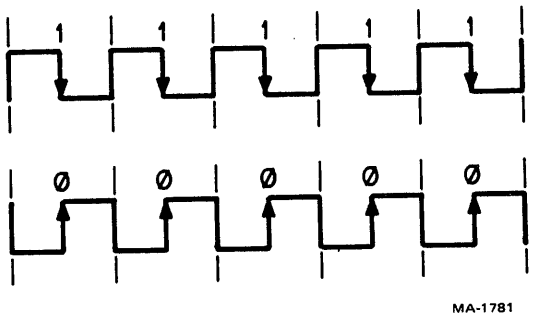
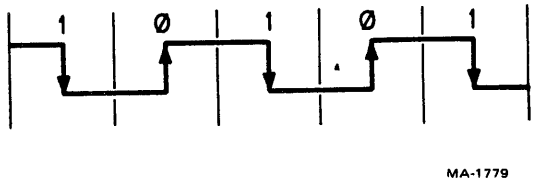


Figure C-1 NRZI Format (Nine-channel)



a. Sequential 1s and Sequential 0s



b. Alternate 1s and 0s

Figure C-2 PE Waveforms

The PE read electronics uses a data window to isolate data transitions (Figure C-3). Zeros in the preamble are used to set the window in position when reading in a forward direction, while 0s in the postamble perform this function when reading in the reverse direction. The all-1s character in the preamble and postamble is used to mark the beginning of data.

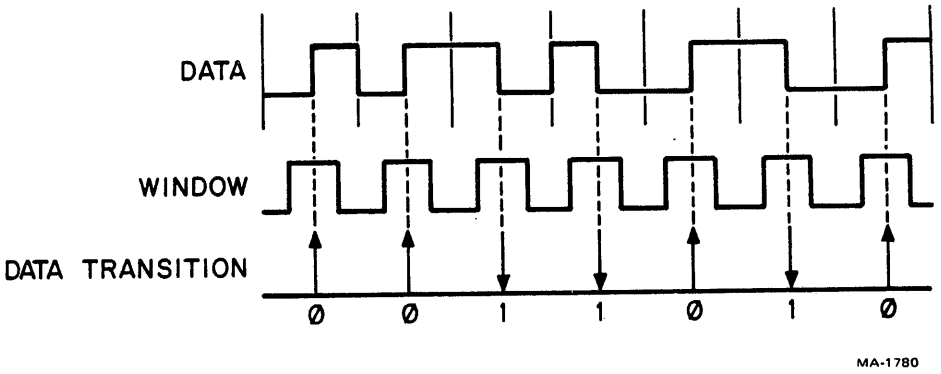


Figure C-3 Data Window

Tape Mark – A PE tape mark consists of forty 0s in tracks 1, 2, 4, 5, 7, and 8 (bit positions 0, 1, 2, 5, 7, and 8) with tracks 3, 6, and 9 (bit positions 4, 6, and 3) dc erased.

Identification Burst (IDB) – The IDB identifies the tape as being a PE tape. It consists of alternating 1s and 0s in the parity track (track 4) with all other tracks erased. The IDB is located at BOT, and has a minimum length of 4.3 cm (1.7 in.). Figure C-4 illustrates PE tape format.

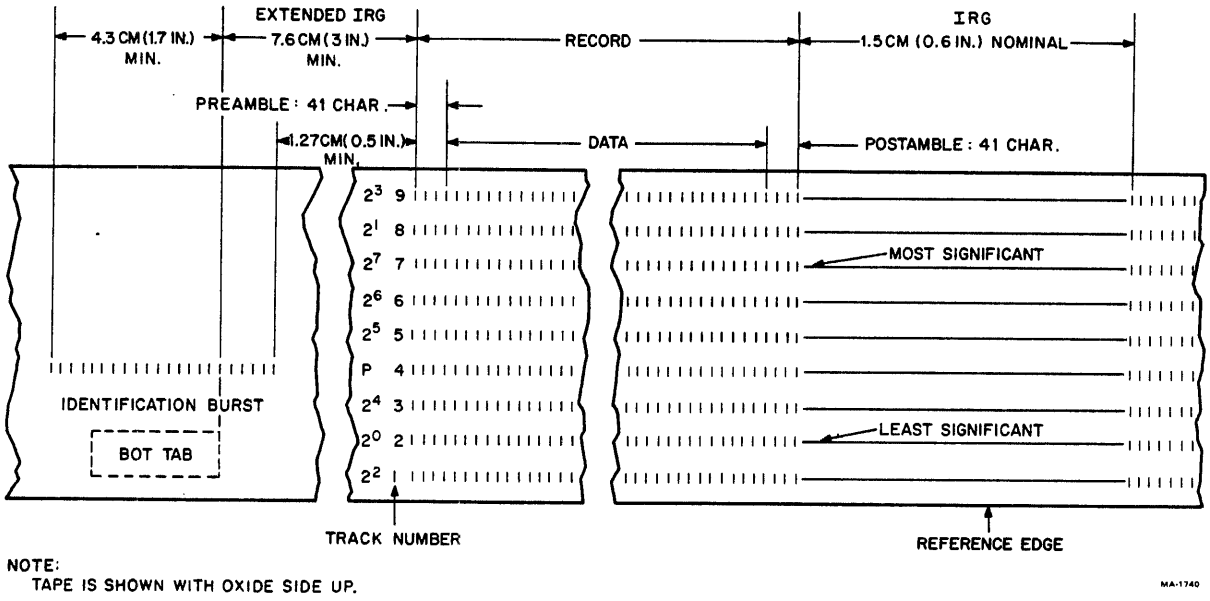


Figure C-4 PE Recording Format

C.2.3 PE Characteristics

Phase encoding, also referred to as Manchester, Williams, Ferranti method for phase modulation, is currently used in high-density (1000–2000 bit per inch) magnetic tape stores. A cell is occupied by a square wave with one cell period. The usual convention is that it represents a logical 0 if the first half of the square-wave is positive and the second half is negative; for a logical 1 it is the opposite. Worded slightly differently, a positive-to-negative transition, in the middle of a cell, represents a logical 0, and a flux transition from negative to positive, in the middle of a cell, signifies a logical 1. If two identical symbols – two logical 0s or two logical 1s – follow each other, there is an interbit flux transition at the boundary of the cell. This interbit flux transition will be ignored by the readback circuitry. PE is self-clocking as there is always a flux transition per cell.

Comparing NRZI with PE, it would appear at first that as phase modulation requires more transitions per bit than NRZI, it would permit lower maximum bit density. However, there are more important considerations. In NRZI coding, the spacing of subsequent transitions may vary from a minimum determined by the chosen bit density for a string of logical 1s to a large value for a long string of 0s. This random variation of transitions causes peak shift and amplitude fluctuations. In a phase-encoded system, the ratio of maximum to minimum spacing is 2. Hence, although pulse crowding and peak shift phenomena in a system that has fixed magnetic and mechanical parameters are reached at a lower bit packing density with PE than with NRZI coding, the peak shift and amplitude fluctuation in PE are well defined and constant.

The comparison of the frequency spectra of NRZI and PE systems reveals another important difference between the two. The noise spectrum of a practical system (where the term "noise" includes all unwanted signals, not only random noise) exhibits large peaks at the low frequency end. Although the highest frequency in a PE system is twice that of the corresponding NRZI, the required band does not extend to low frequencies and a better signal-to-noise ratio can be achieved.

With respect to the coding system's sensitivity to read errors, some broad qualitative conclusions are obtained. If in an NRZI coding system a single 1 or a single 0 is misread, it will have no effect on the interpretation of the forthcoming data bits of the sequence. [As NRZI is not self-clocking, in a parallel-recording multitrack system each character must have at least one low-transition (i.e., logical 1) in it from which the read clock is derived.]

In a typical phase-encoded readback channel, the read clock is derived from the data flux transition. The read logic separates the bit flux transitions which occur in the middle of the cell from the interbit transitions at the cell boundaries by opening a "window" at the expected bit transition time (Figure C-3). The possible consequences of a single-bit dropout are illustrated in Figure C-5. It is assumed that the dropout occurs in the position of a bit-transition in a long chain of logical 1s. The interbit transition following the dropout will now generate the next clock pulse and the subsequent logical 1s are misread until synchronism is regained. Thus a single bit-transition dropout can cause an "error burst" extending over many bit lengths. In actual systems the possibility of this type of error is avoided by provision of a phase-lock oscillator which is normally resynchronized at every bit flux transition, but can maintain synchronism over a certain number of bits without re-synchronization.

The checklist of PE reads is as follows.

1. Efficiency is low (50 percent). There are two flux reversals per bit.
2. Correlation is good; there is the maximum possible difference between logical 0 and 1.
3. Bandwidth requirement is fair, does not extend to low frequencies, but maximum frequency is twice that of NRZI at the same density.
4. The system is self-clocking.

5. Read resolution is poor, limited to a half-bit period.

6. Circuit complexity is higher than for NRZI.

7. Noise immunity is good; peak shift and amplitude fluctuation is predictable and constant at any one recording density.

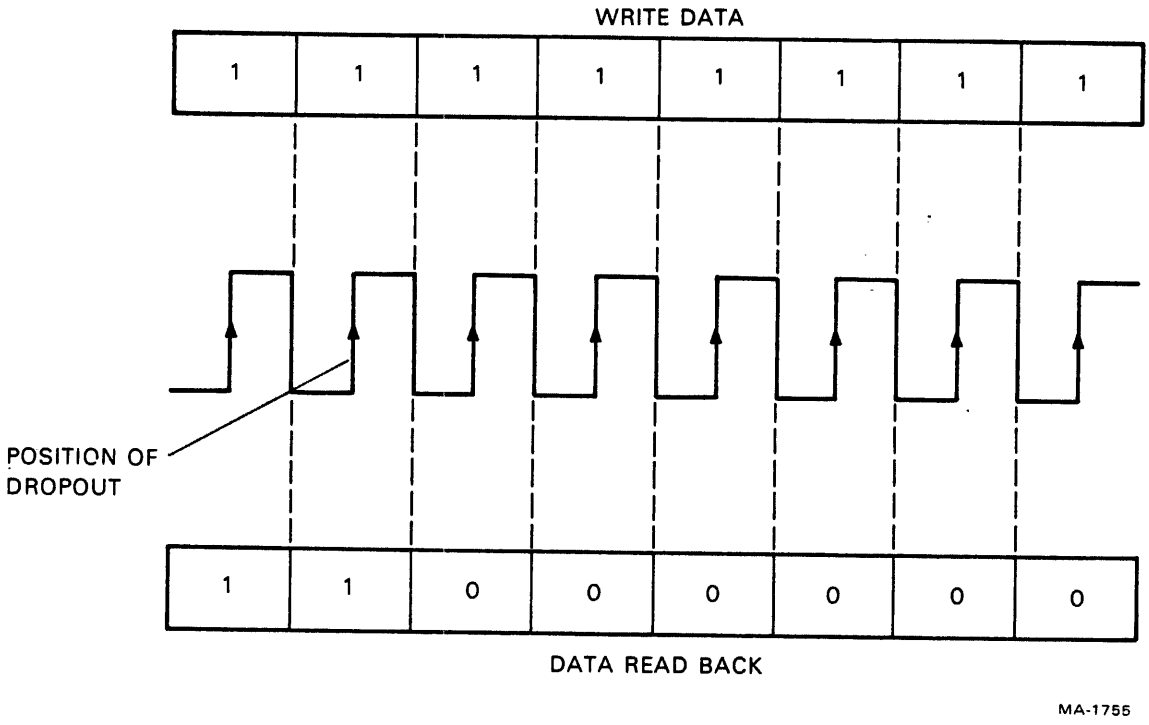


Figure C-5 Potential Error Caused by Single Bit Dropout in PE

The phase-encoded format (Figure C-4) does not utilize the CRC and LRC characters for error checking. Each data block is preceded by 40 all-0s bytes followed by a single all-1s byte (preamble) and is terminated by a single all-1s byte followed by 40 all-0s bytes (postamble). The preamble synchronizes the read detection circuits so that 1s and 0s are correctly identified in the data bytes which follow. The symmetry of preamble and postamble permits reading in either direction. At the load point (beginning of tape), an "identification burst" consisting of 1600 flux reversals per inch, is written in the parity track. Odd character parity is specified. The tape mark consists of 64 to 256 flux reversals at 3200 flux changes per inch in tracks 1, 2, P, 5, 7, 8. The remaining tracks are dc erased.

In phase-encoded systems there is, contrary to NRZI coding, a continuous readback signal which, because of the bandwidth limitation of the record/reproduce chain and the inherent properties of the recording media, appears as a near-sinusoidal signal. In high-density phase-encoded systems, the zero-crossings of this quasi-sinusoidal signal can be used for accurate location of the readback pulse. This detection system is used for some single-track serial recordings.

APPENDIX D
TM03 INTERFACE SIGNALS

Table D-1 M5903/Massbus Interface Signals

Cable	Pin*		Polarity	Signal
Cable A	A	1	−	MASS D00
	B	2	+	
	C	3	+	MASS D01
	D	4	−	
	E	5	−	MASS D02
	F	6	+	
	H	7	+	MASS D03
	J	8	−	
	K	9	−	MASS D04
	L	10	+	
	M	11	+	MASS D05
	N	12	−	
	P	13	−	MASS C00
	R	14	+	
	S	15	+	MASS C01
	T	16	−	
	U	17	−	MASS C02
	V	18	+	
	W	19	+	MASS C03
	X	20	−	
	Y	21	−	MASS C04
	Z	22	+	
	AA	23	+	MASS C05
	BB	24	−	
	CC	25	−	MASS SCLK
	DD	26	+	
	EE	27	+	MASS RS3
	FF	28	−	
	HH	29	+	MASS ATTN
	JJ	30	−	
	KK	31	−	MASS RS4
	LL	32	+	
	MM	33	−	MASS CTOD
	NN	34	+	

*Pin designations may be letters or numerals.

Table D-1 M5903/Massbus Interface Signals (Cont)

Cable	Pin*		Polarity	Signal
Cable A (cont)	PP	35	+	MASS WCLK
	RR	36	−	
	SS	37	+	MASS RUN
	TT	38	−	
	UU	39		SPARE
	VV	40		GND
Cable B	A	1	−	MASS D06
	B	2	+	
	C	3	+	MASS D07
	D	4	−	
	E	5	−	MASS D08
	F	6	+	
	H	7	+	MASS D09
	J	8	−	
	K	9	−	MASS D10
	L	10	+	
	M	11	+	MASS D11
	N	12	−	
	P	13	−	MASS C06
	R	14	+	
	S	15	+	MASS C07
	T	16	−	
	U	17	−	MASS C08
	V	18	+	
	W	19	+	MASS C09
	X	20	−	
	Y	21	−	MASS C10
	Z	22	+	
	AA	23	+	MASS C11
	BB	24	−	
	CC	25	−	MASS EXC
	DD	26	+	
	EE	27	+	MASS RS0
	FF	28	−	
	HH	29	+	MASS EBL
	JJ	30	−	
	KK	31	−	MASS RS1
	LL	32	+	
	MM	33	−	MASS RS2
	NN	34	+	
	PP	35	+	MASS INIT
	RR	36	−	
	SS	37	+	MASS SP1
	TT	38	−	
	UU	39		SPARE
	VV	40		GND

*Pin designations may be letters or numerals.

Table D-1 M5903/Massbus Interface Signals (Cont)

Cable	Pin*		Polarity	Signal
Cable C	A	1	–	MASS D12
	B	2	+	
	C	3	+	MASS D13
	D	4	–	
	E	5	–	MASS D14
	F	6	+	
	H	7	+	MASS D15
	J	8	–	
	K	9	–	MASS D16
	L	10	+	
	M	11	+	MASS D17
	N	12	–	
	P	13	–	MASS DPA
	R	14	+	
	S	15	+	MASS C12
	T	16	–	
	U	17	–	MASS C13
	V	18	+	
	W	19	+	MASS C14
	X	20	–	
	Y	21	–	MASS C15
	Z	22	+	
	AA	23	+	MASS CPA
	BB	24	–	
	CC	25	–	MASS OCC
	DD	26	+	
	EE	27	+	MASS DS0
	FF	28	–	
	HH	29	+	MASS TRA
	JJ	30	–	
	KK	31	–	MASS DS1
	LL	32	+	
	MM	33	–	MASS DS2
	NN	34	+	
	PP	35	+	MASS DEM
	RR	36	–	
	SS	37	+	MASS SP2
	TT	38	–	
	UU	39	H	MASS FAIL
	VV	40		GND

*Pin designations may be letters or numerals.

Table D-2 M8937/Slave Bus Interface Signals

Connector	Pin	Signal	Connector	Pin	Signal
J1	A	WD0 (SB)L	J1 (cont)	B	GND
	C	WDP (SB)L		D	
	E	WD1 (SB)L		F	
	H	WD7 (SB)L		J	
	K	WD2 (SB)L		L	
	M	WD6 (SB)L		N	
	P	REC (SB)L		R	
	S	ACCL (SB)L		T	
	U	SS1 (SB)L		V	
	W	LRC STRB (SB)L		X	
	Y	SS2 (SB)L		Z	
	AA	WD5 (SB)L		BB	
	CC	WD4 (SB)L		DD	
	EE	WD3 (SB)L		FF	
	HH	SS0 (SB)L		JJ	
	KK	SLAVE SET PLS (SB)L		LL	
	MM	EMD (SB)L		NN	
	PP	INIT PLS (SB)L		RR	
	SS	DRV CLR PLS (SB)L		TT	
	UU	STOP (SB)L			
	VV	+5 V			

Table D-3 M8908-YA/Slave Bus Interface Signals

Connector	Pin	Signal	Connector	Pin	Signal
J1	A	RD0 (SB)L	J1 (cont)	UU	REV (SB)L
	C	RDP (SB)L		VV	+5 V
	E	RD1 (SB)L		B	GND
	H	RD7 (SB)L		D	
	K	RD2 (SB)L		F	
	M	RD6 (SB)L		J	
	P	RD3 (SB)L		L	
	S	RD5 (SB)L		N	
	U	RD4 (SB)L		R	
	W	RSDO (SB)L		T	
	Y	BOT (SB)L		V	
	AA	END PT (SB)L		X	
	CC	SET SSC (SB)L		Z	
	EE	RWND (SB)L		BB	
	HH	SET VPE (SB)L		DD	
	KK	TUR (SB)L		FF	
	MM	TAPE WRT CLK (SB)L		JJ	
	PP	FWD (SB)L		LL	
	RR	CLOCK (SB)L		NN	
	SS	WRITE (SB)L		TT	

Table D-4 M8908/Slave Bus Interface Signals

Connector	Pin	Signal	Connector	Pin	Signal
J1	A	MOL (SB)L	J1 (cont)	AA	DT1 (SB)L
	B	PESB (SB)L		CC	WRL (SB)L
	C	7CH (SB)L		EE	BUS 1600 BPI L (DEN0 (SB)L)
	D	SN00 (SB)L		HH	DT0 (SB)L
	E	SN02 (SB)L		KK	SDWN (SB)L
	F	SN05 (SB)L		MM	SLA (SB)L
	H	SN04 (SB)L		PP	IRD (SB)L
	J	SN06 (SB)L		RR	SPR (SB)L
	K	SN01 (SB)L		SS	1600 BPI L (DEN2 (SB)L)
	L	SN07 (SB)L		UU	1600 BPI H (DEN1 (SB)L)
	M	SN08 (SB)L		VV	+5 V
	N	SN09 (SB)L		Z	GND
	P	SN10 (SB)L		BB	
	R	SN11 (SB)L		DD	
	S	SN12 (SB)L		FF	
	T	SN13 (SB)L		JJ	
	U	SN14 (SB)L		LL	
	V	SN15 (SB)L		NN	
	W	SN03 (SB)L		TT	
	X	DT2 (SB)L			
	Y	RWS (SB)L			

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EK-0TM03-TM-002

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